NAND Flash Memory - FortisFlash™

MT29F512G08EBLEE, MT29F1T08EELEE, MT29F2T08EMLEE MT29F4T08EULEE, MT29F8T08EWLEE

B47R FortisFlash™ Features

- Open NAND Flash Interface (ONFI) 4.2-compliant[1]
- JEDEC NAND Flash Interoperability (JESD230D) compliant[2]
- Triple-level cell (TLC)
- Organization
  - Page size x8: 18,352 bytes (16,384 + 1968 bytes)
  - Block size: 2112 pages, (33,792K + 4059K bytes)
  - Plane size: 4 planes x 556 blocks
  - Device size: 512Gb: 2224 blocks; 1Tb: 4448 blocks; 2Tb: 8896 blocks; 4Tb: 17,792 blocks, 8Tb: 35,584 blocks
- NV-DDR3 I/O performance[6]
  - Up to NV-DDR3 timing mode 15
  - Clock rate: 1.25ns (NV-DDR3)
  - Read/write throughput per pin: 1.6 GT/s
- TLC Array performance
  - IWL READ operation time: 47us (TYP)
  - READ PAGE operation time: 52us (TYP)
  - Effective Program page time: 500us (TYP)
  - Erase block time: 5ms (TYP)
- Operating Voltage Range
  - V_{CC}: 2.35–3.6V
  - V_{CCQ}: 1.14–1.26V
- Command set: ONFI NAND Flash Protocol

- Data is required to be randomized by the external host prior to being inputted to the NAND device, see External Data Randomizaiton
- First block (block address 00h) is valid when shipped from factory. For minimum required ECC, see Error Management.[5]
- RESET (FFh) required as first command after power-on
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Copyback operations supported within the plane from which data is read
- On-die Termination (ODT)[3]
- Quality and reliability[4]
  - Testing methodology: JESD47
  - Data retention: See qualification report – May vary for targeted application
  - TLC Endurance: 3000 PROGRAM/ERASE cycles
  - SLC Endurance: 60,000 PROGRAM/ERASE cycles
- This device is not intended for use in applications that require data to be pre-programmed in the NAND array prior to Reflow, Surface Mount, or any thermal processing. Please contact your Micron representative for details.
- Operating temperature:
  - Commercial: 0°C to +70°C
- Package
  - 132-ball BGA

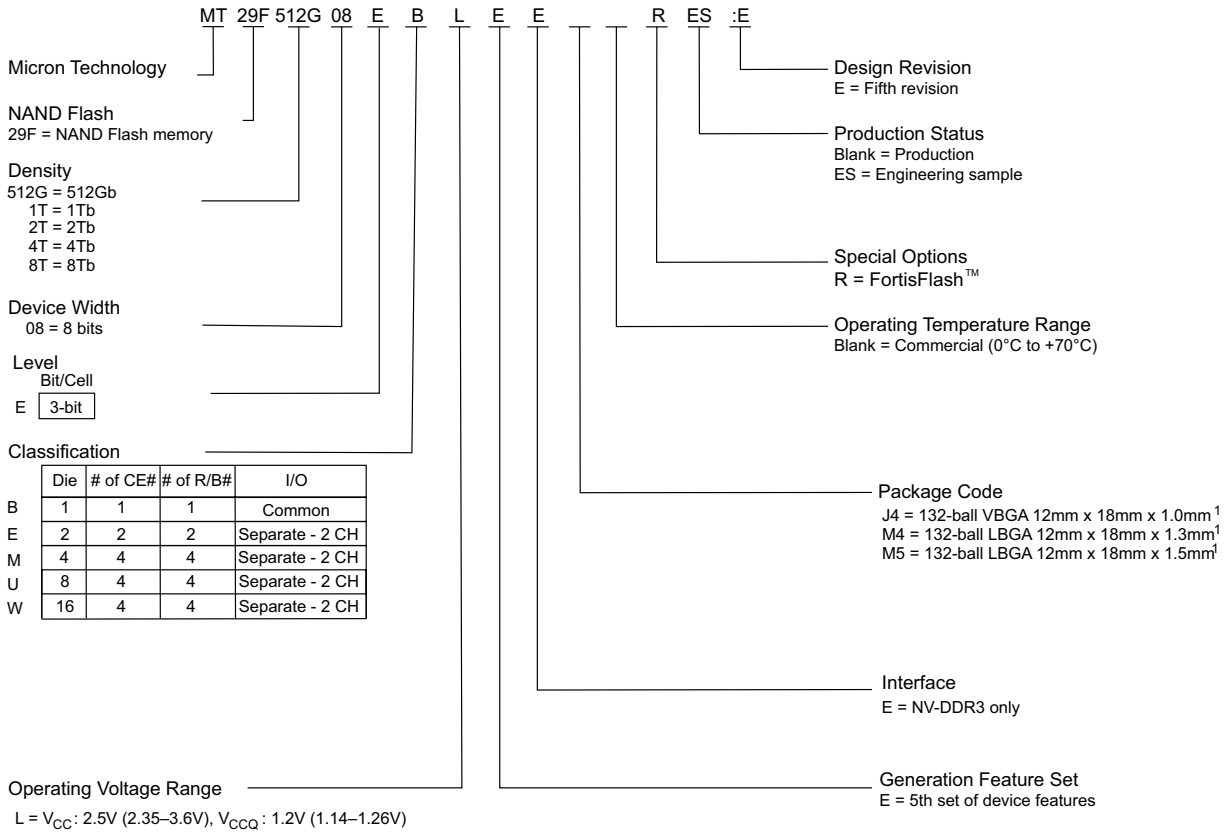
Notes: 1. The ONFI 4.2 specification is available at www.onfi.org.
2. The JEDEC specification is available at www.jedec.org/standards-documents.
3. ODT functionality is supported.
4. Read Retry operations and Auto Read Calibration operations are required to achieve specified endurance and for general array data integrity.
5. For minimum required ECC, see Error Management section.
6. The I/O performance quoted only applies to NAND packages and channel topologies with up to 4 die per channel load. The 16-die 2-channel package only supports up to 1200 MT/s. The maximum data rate the actual system can achieve however, depends heavily on the user's board design and topology. Thus, the user must determine whether their system can achieve the desired data rate through signal integrity simulations and analysis.

Release: 8/26/2021

Part Numbering Information

Micron NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Numbering Information



Note: 1. All packages are Pb-free.

Figure 2: B47R Part Numbering Summary Table

Device	# of Die	Density	# of CE #	# of R/B #	I/O	Package	Thickness
MT29F512G08EBLEEJ4	1	512Gb	1	1	Common	132-ball VBGA	1.0 mm
MT29F1T08EELEEJ4	2	1Tb	2	2	Separate 2 CH	132-ball VBGA	1.0 mm
MT29F2T08EMLEEJ4	4	2Tb	4	4	Separate 2 CH	132-ball VBGA	1.0 mm
MT29F4T08EULEEM4	8	4Tb	4	4	Separate 2 CH	132-ball LBGA	1.3 mm
MT29F8T08EWLEEM5	16	8Tb	4	4	Separate 2 CH	132-ball LBGA	1.5 mm

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General Description

Micron NAND devices use a highly multiplexed 8-bit bus (DQx) to transfer commands, address, and data. There are five control signals used to implement in the data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

This Micron NAND Flash device includes a NV-DDR3 data interface for high-performance I/O operations. Data transfers include a bidirectional data strobe (DQS).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). For further details, see Device and Array Organization.

NV-DDR3 Signal Descriptions

Table 1: NV-DDR3 Signal Definitions

NV-DDR3 Signal[1]	Type	Description[2]
ALE	Input	**Address latch enable:**Loads an address from DQx into the address register.
CE#	Input	**Chip enable:** Enables or disables one or more die (LUNs) in a target.
CLE	Input	**Command latch enable:** Loads a command from DQx into the command register.
DQx	I/O	**Data inputs/outputs:** The bidirectional I/Os transfer address, data, and command information.
DQS, DQS_t	I/O	**Data strobe:** Provides a synchronous reference for data input and output.
DQS_c	I/O	**Data strobe complement:** Provides a complementary signal to the data strobe signal optionally used for reference for data input and output.
RE#, RE_t	Input	**Read enable:** RE# transfers serial data from the NAND Flash to the host system.
RE_c	Input	**Read enable complement:** Provides a complementary signal to the read enable signal optionally used for reference for data output.
WE#	Input	**Write enable:** WE# transfers commands, addresses.
WP#	Input	**Write protect:** Enables or disables array PROGRAM and ERASE operations.
R/B#	Output	**Ready/busy:** An open-drain, active-low output that requires an external pull-up resistor. This signal indicates target array activity.
V_{CC}	Supply	**V_{CC}:** Core power supply
V_{CCQ}	Supply	**V_{CCQ}:** I/O power supply
V_{PP}	Supply	**V_{PP}:** The V_{PP} signal is an optional external high voltage power supply to the device. This high voltage power supply may be used to enhance operations (for example, improved power efficiency). If V_{PP} will not be utilized by a host system, that V_{PP} signal location is then defined as a DNU signal location.
V_{SS}	Supply	**V_{SS}:** Core ground connection
V_{SSQ}	Supply	**V_{SSQ}:** I/O ground connection
V_{REFQ}	Supply	**V_{REFQ}**: Reference voltage

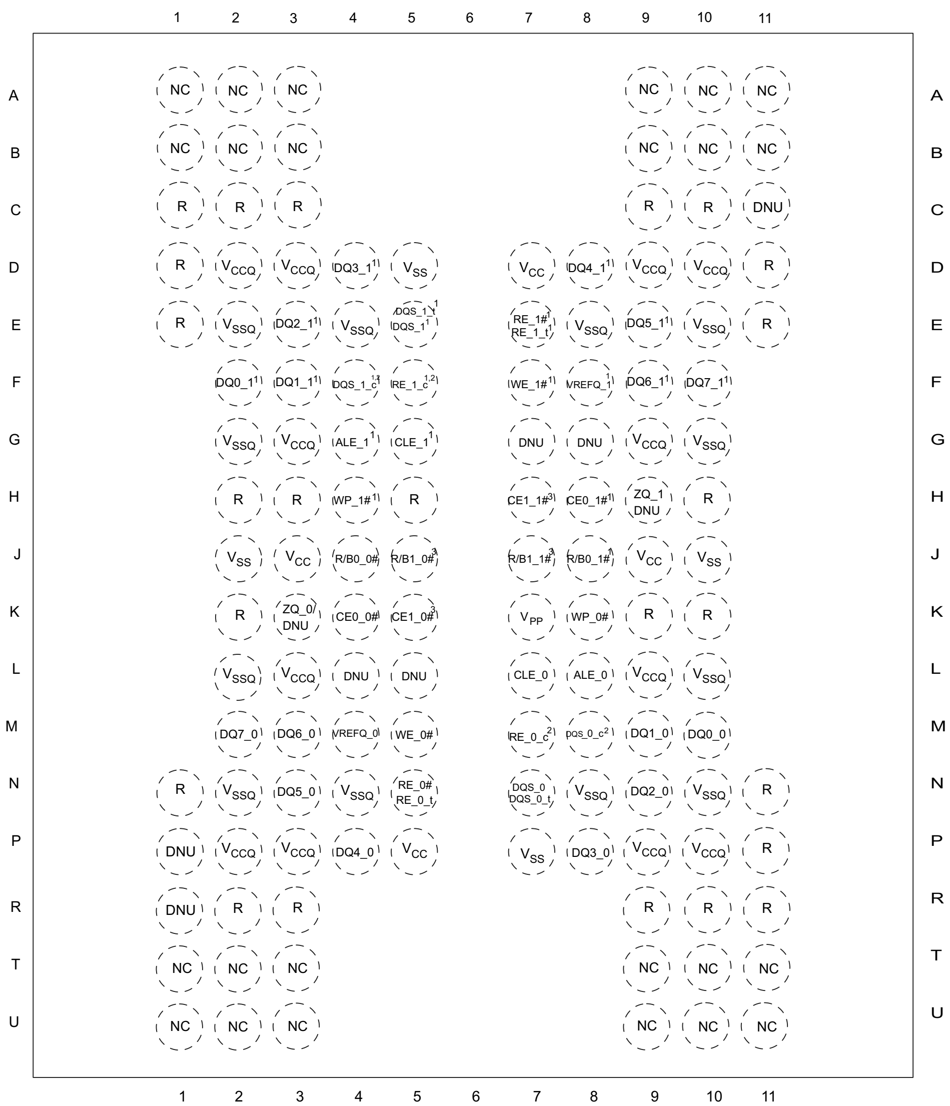
Table 1: NV-DDR3 Signal Definitions (Continued)

NV-DDR3 Signal[1]	Type	Description[2]
ZQ	–	**Reference pin for ZQ calibration**: This is used on ZQ calibration. The ZQ signal shall be connected to Vss through R_{ZQ} resistor.
NC	–	**No connect:** NCs are not internally connected. They can be driven or left unconnected.
DNU	–	**Do not use:** DNUs must be left unconnected.
RFU	–	**Reserved for future use:** RFUs must be left unconnected.

Notes: 1. See Device and Array Organization and Signal Assignment sections for detailed signal connections.
2. See Bus Operation – NV-DDR3 Interface for detailed signal descriptions.

Signal Assignments

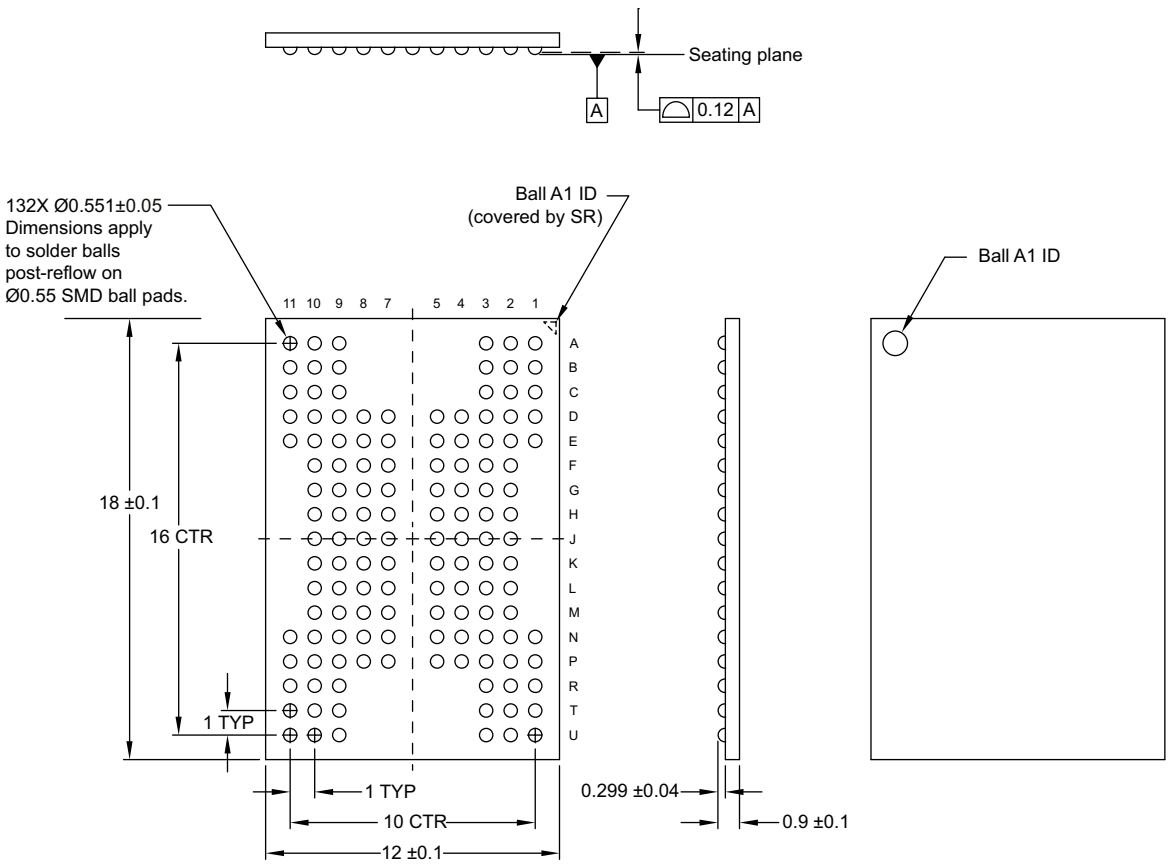
Figure 3: 132-ball BGA (Ball-Down, Top View)



Notes: 1. These signals are available on dual, quad, octal or higher die stacked die packages. They are NC for other configurations.
2. These signals are available when differential signaling is enabled.
3. These signals are available on quad die four CE#, octal die, or 16 die stacked packages. They are NC for other configurations.

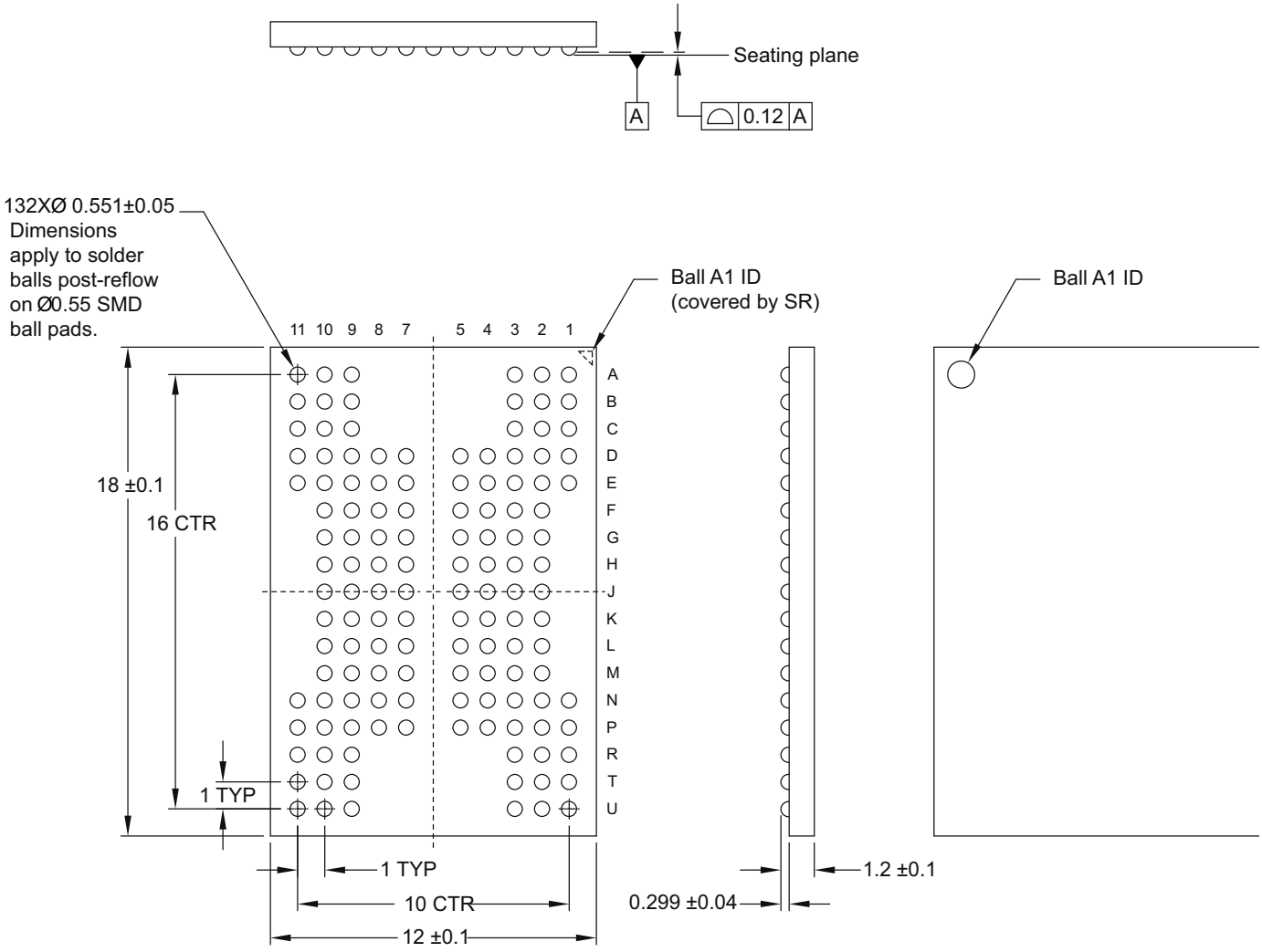
Package Dimensions

Figure 4: 132-Ball VBGA – 12mm x 18mm x 1.0 (Package Code: J4)



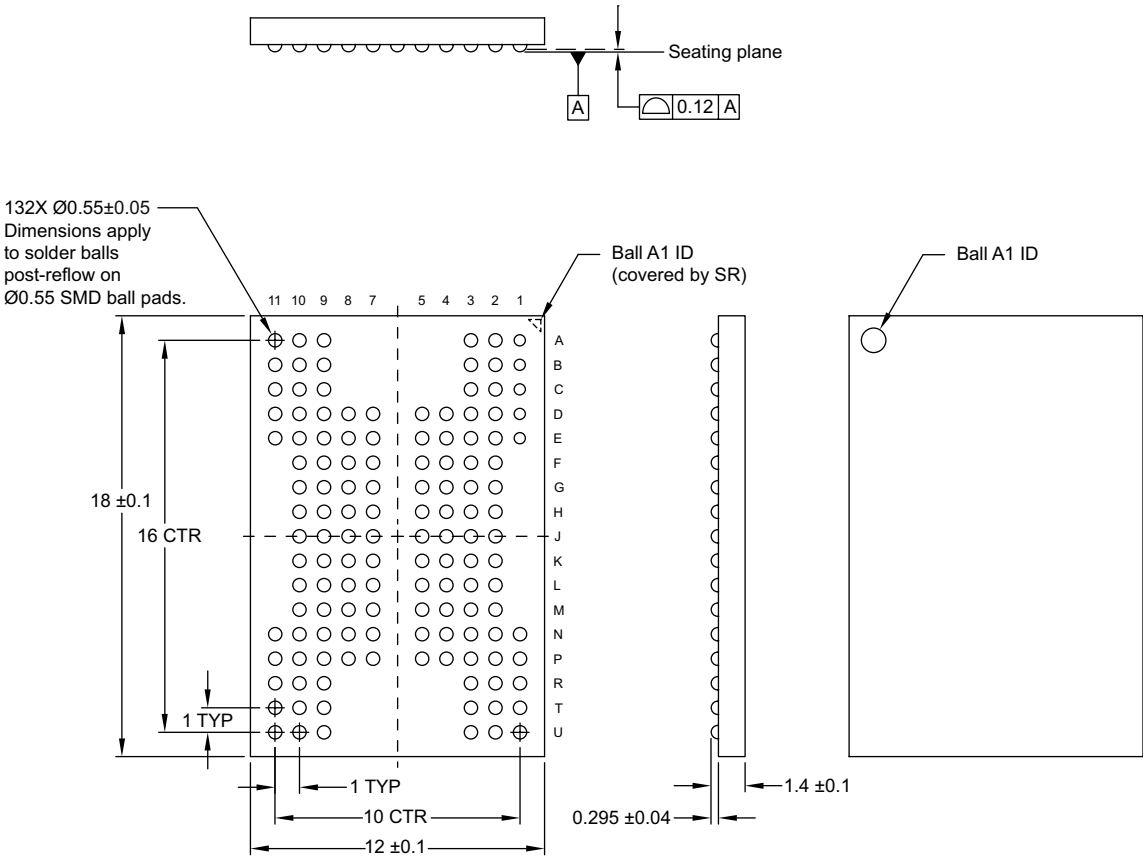
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SACQ (92.45% Sn, 4.0% Ag, 3.0% Bi, 0.5% Cu, 0.05% Ni).

Figure 5: 132-Ball LBGA – 12mm x 18mm x 1.3 (Package Code: M4)



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SACQ (92.45% Sn, 4.0% Ag, 3.0% Bi, 0.5% Cu, 0.05% Ni).

Figure 6: 132-Ball LBGA – 12mm x 18mm x 1.5 (Package Code: M5)



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SACQ (92.45% Sn, 4.0% Ag, 3.0% Bi, 0.5% Cu, 0.05% Ni).

Architecture

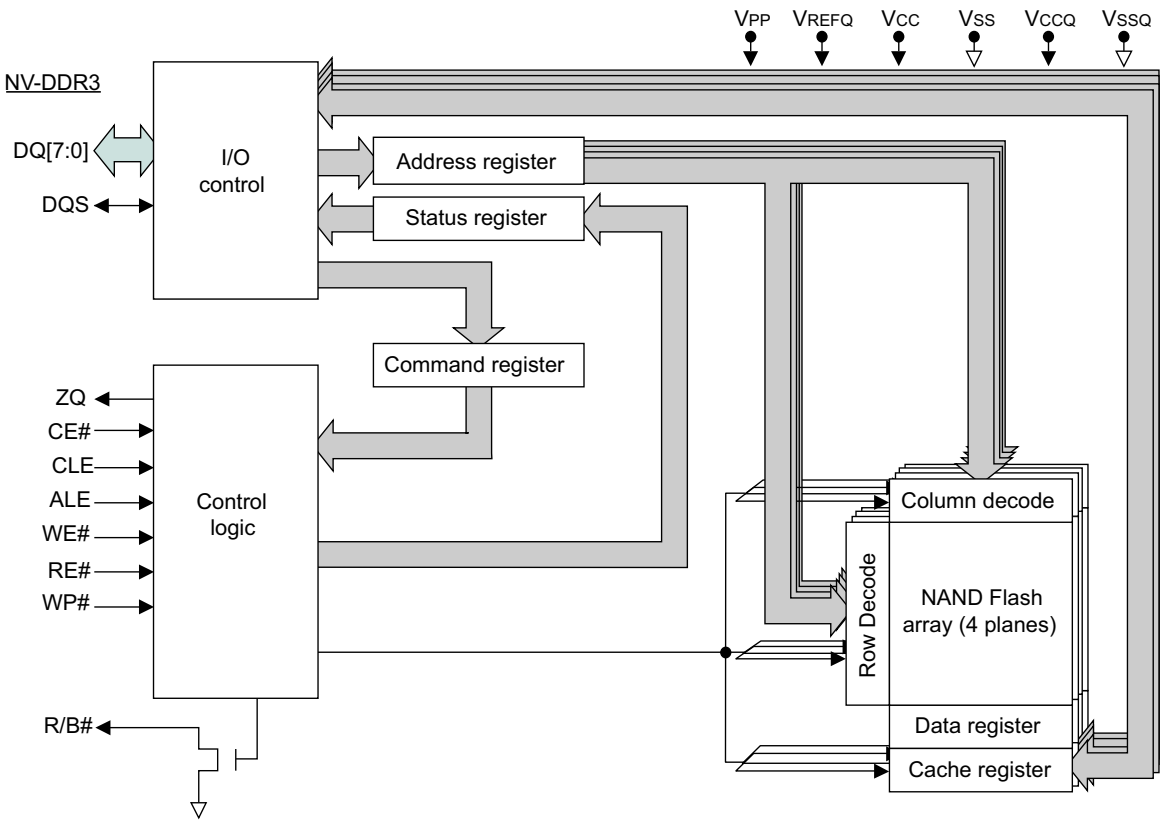
These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte by byte, through a data register and a cache register.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput.

The status register reports the status of die (LUN) operations.

Figure 7: NAND Flash Die (LUN) Functional Block Diagram



Device and Array Organization

Figure 8: Device Organization for Single-Die Package (132-ball BGA)

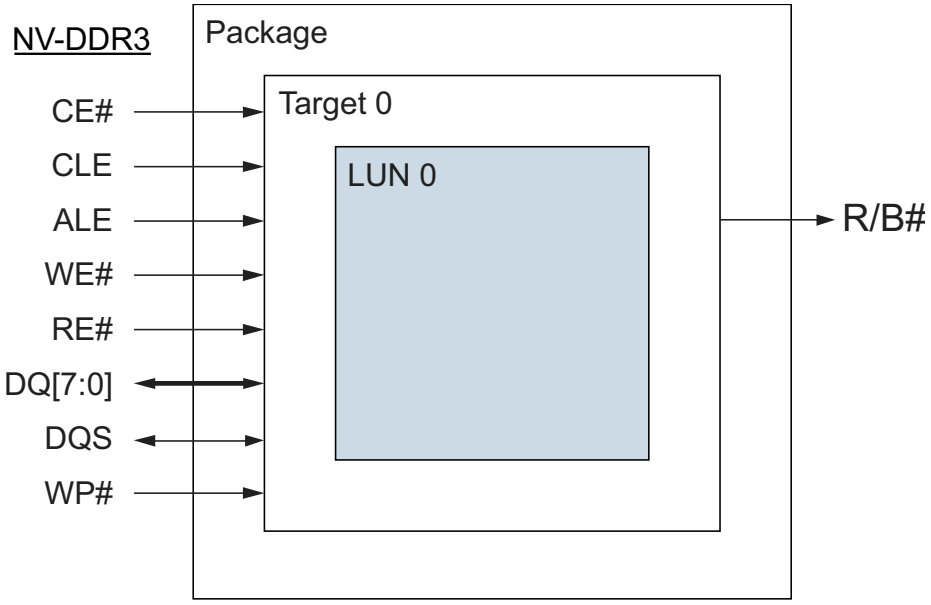


Figure 9: Device Organization for Two-Die Package (132-ball BGA)

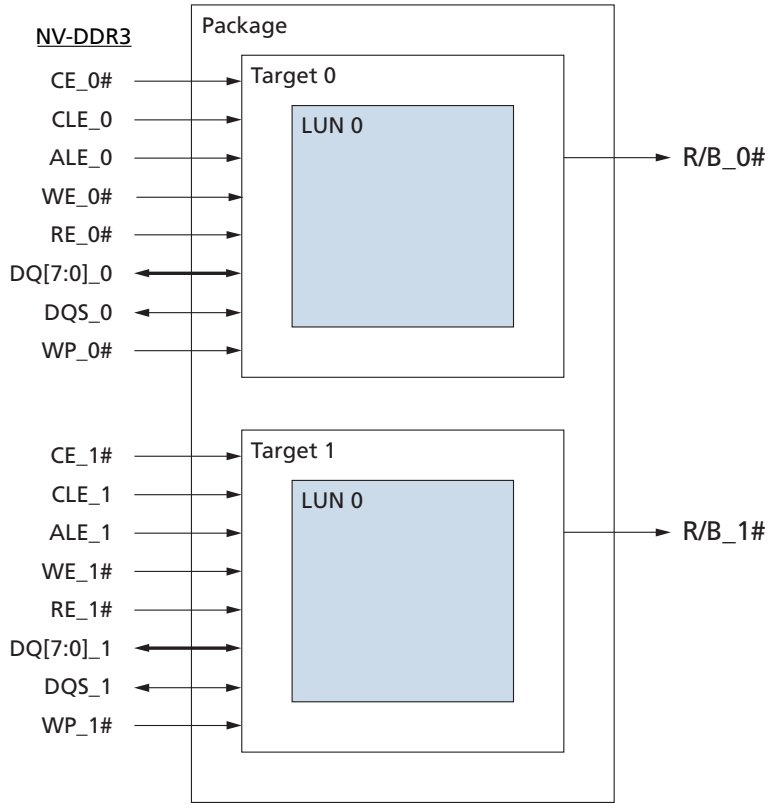


Figure 10: Device Organization for Four-Die Package (132-ball BGA)

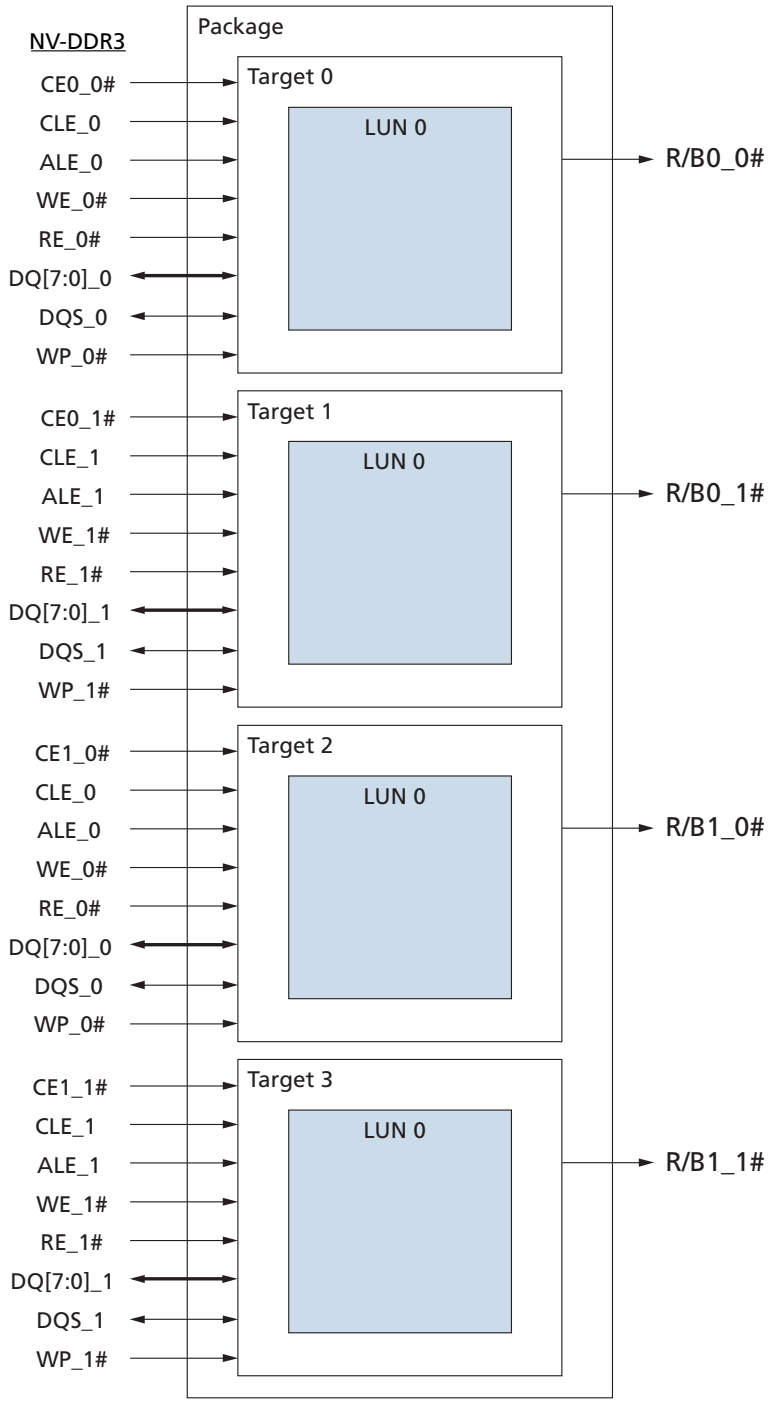


Figure 11: Device Organization for Eight-Die Package (132-ball BGA)

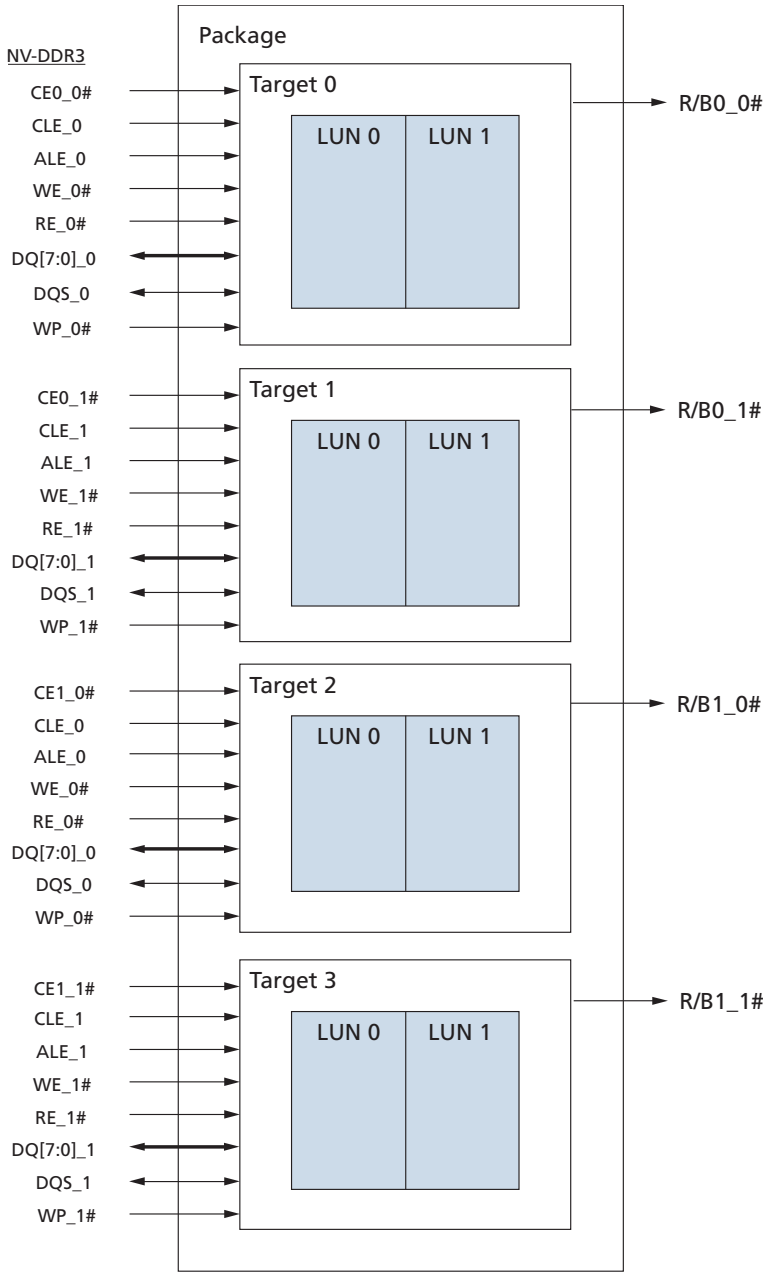


Figure 12: Device Organization for Sixteen-Die Package (132-ball BGA)

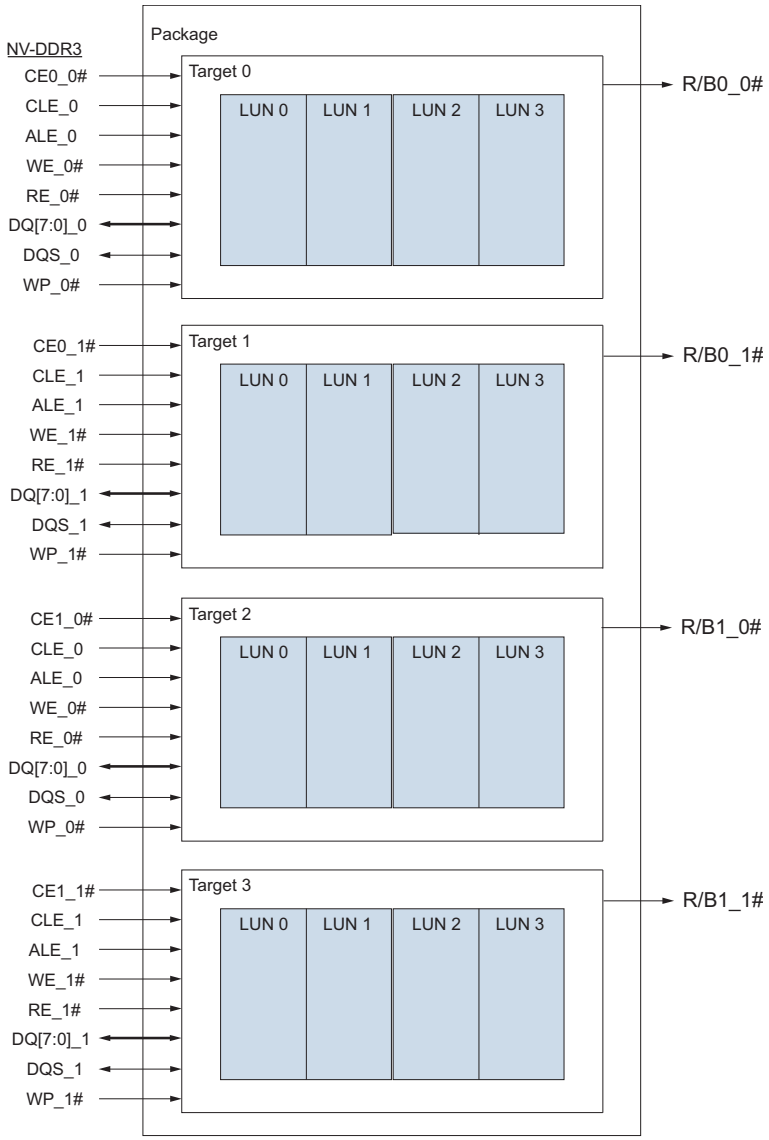


Figure 13: Array Organization per Logical Unit (LUN) for B47R in TLC mode

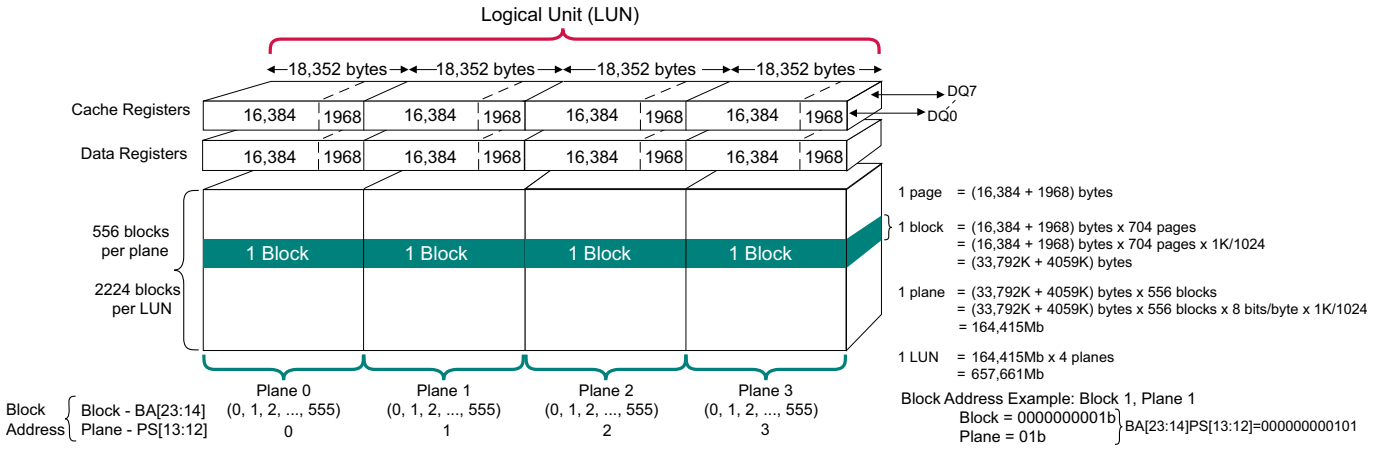


Table 2: Array Addressing for Logical Unit (LUN) for B47R in TLC mode

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0[2]
Second	LOW	CA14[3]	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	PS13[5]	PS12[5]	PA11[4]	PA10	PA9	PA8
Fifth	BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16
Sixth	LOW	LOW	LOW	LOW	LOW	LOW	LA1[6,7]	LA0[6,7]

Notes: 1. CAx = column address, PAx = page address, PSx = plane select, BAx = block address, LAx = LUN address; the page address, plane select, block address, and LUN address are collectively called the row address. Consequently, the first and second cycles containing the column addresses are known as C1 and C2, and the third, fourth, fifth, and sixth cycles containing the row addresses cycles are known as R1, R2, R3, and R4 respectively.

2. For NV-DDR3 interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
3. CA [14:0] address column addresses 0 through 18,351 (16,384 + 1968) (47AFh), therefore column addresses 18,352 (47B0h) through 32,767 (7FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
4. PA [11:0] address page addresses 0 through 2111 (83Fh), therefore page addresses 2112 (840h) through 4095 (FFFh) are invalid, out of bounds, and do not exist in the device. It is not allowed to issue any PROGRAM, READ, ERASE, or any other array operation on out of bounds pages.
5. PS[13:12] are the plane-select bits:
   Plane 0: PS[13:12] = 00b
   Plane 1: PS[13:12] = 01b
   Plane 2: PS[13:12] = 10b
   Plane 3: PS[13:12] = 11b
6. LA0, LA1 are the LUN-select bits. They are present only when two or more LUNs are shared on the target; otherwise, they should be held LOW.
   LUN 0: LA0 = 0, LA1 = 0
   LUN 1: LA0 = 1, LA1 = 0
   LUN 2: LA0 = 0, LA1 = 1
   LUN 3: LA0 = 1, LA1 = 1
   The sixth address cycle is required for all LUN per Target (CE#) configurations (i.e. 1, 2, and 4 LUNs per CE#) regardless if a LUN-select bit is present in the sixth address cycle. If there is no LUN-select bit present in the sixth address cycle then the sixth address cycles is required to be 00h.
7. For single LUN Targets block addresses 2224 through 4095 are invalid, out of bounds, and do not exist in the device. For two LUN Targets block addresses 2224 through 4095 and 6320 through 8191 are invalid, out of bounds, and

do not exist in the device.
For four LUN Targets block addresses 2224 through 4095, 6320 through 8191, 10,416 through 12,287, and 14,512 through 16,383 are invalid, out of bounds, and do not exist in the device.
It is not allowed to issue any PROGRAM, READ, ERASE, or any other array operation on out of bounds blocks.

Figure 14: Array Organization per Logical Unit (LUN) for B47R in SLC mode

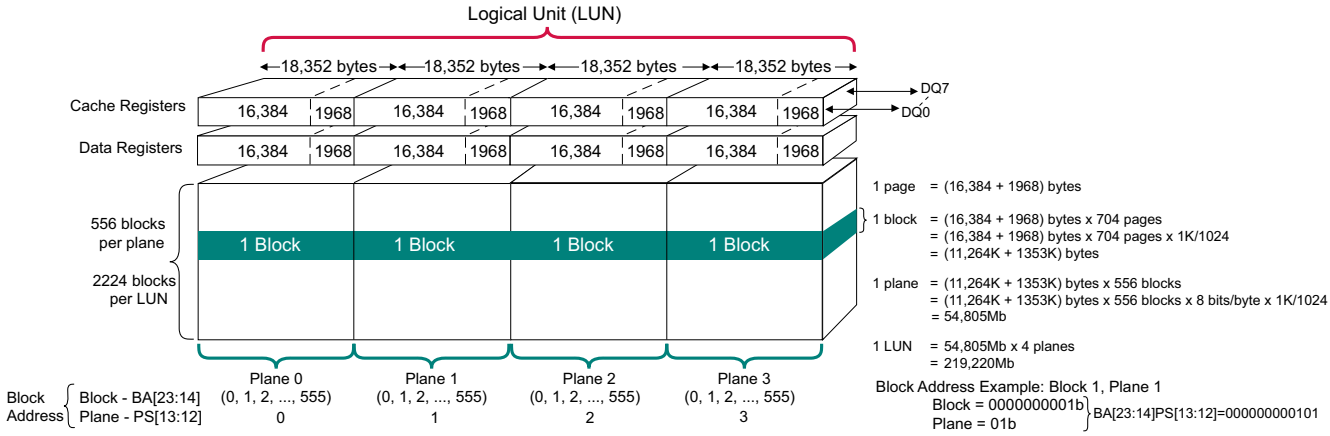


Table 3: Array Addressing for Logical Unit (LUN) for B47R in SLC mode

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0[2]
Second	LOW	CA14[3]	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	PS13[5]	PS12[5]	LOW	LOW	PA9[4]	PA8
Fifth	BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16
Sixth	LOW	LOW	LOW	LOW	LOW	LOW	LA1[6,7]	LA0[6,7]

Notes: 1. CAx = column address, PAx = page address, PSx = plane select, BAx = block address, LAx = LUN address; the page address, plane select, block address, and LUN address are collectively called the row address. Consequently, the first and second cycles containing the column addresses are known as C1 and C2, and the third, fourth, fifth, and sixth cycles containing the row addresses cycles are known as R1, R2, R3, and R4 respectively.

2. For NV-DDR3 interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
3. CA [14:0] address column addresses 0 through 18,351 (16,384 + 1968) (47AFh), therefore column addresses 18,352 (47B0h) through 32,767 (7FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
4. PA [9:0] address page addresses 0 through 703 (2BFh), therefore page addresses 704 (2C0h) through 1023 (3FFh) are invalid, out of bounds, and do not exist in the device. It is not allowed to issue any PROGRAM, READ, ERASE, or any other array operation on out of bounds pages.
5. PS[13:12] are the plane-select bits:
   Plane 0: PS[13:12] = 00b
   Plane 1: PS[13:12] = 01b
   Plane 2: PS[13:12] = 10b
   Plane 3: PS[13:12] = 11b
6. LA0, LA1 are the LUN-select bits. They are present only when two or more LUNs are shared on the target; otherwise, they should be held LOW.
   LUN 0: LA0 = 0, LA1 = 0
   LUN 1: LA0 = 1, LA1 = 0
   LUN 2: LA0 = 0, LA1 = 1
   LUN 3: LA0 = 1, LA1 = 1
   The sixth address cycle is required for all LUN per Target (CE#) configurations (i.e. 1, 2, and 4 LUNs per CE#) regardless if a LUN-select bit is present in the sixth address cycle. If there is no LUN-select bit present in the sixth address cycle then the sixth address cycles is required to be 00h.

7. For single LUN Targets block addresses 2224 through 4095 are invalid, out of bounds, and do not exist in the device.
   For two LUN Targets block addresses 2224 through 4095 and 6320 through 8191 are invalid, out of bounds, and do not exist in the device.
   For four LUN Targets block addresses 2224 through 4095, 6320 through 8191, 10,416 through 12,287, and 14,512 through 16,383 are invalid, out of bounds, and do not exist in the device.
   It is not allowed to issue any PROGRAM, READ, ERASE, or any other array operation on out of bounds blocks.

Bus Operation – NV-DDR3 Interface

The NV-DDR3 interface is capable of high-speed DDR data transfers and the DQS signal is enabled. DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

Use of differential signaling, external V_{REFQ}, and ZQ calibration is optional for interface speeds 200 MT/s or slower. Differential signaling and external V_{REFQ} are optional for NV-DDR3 interface speeds faster than 200 MT/s but required to guarantee specified AC timings. If a host does not use differential signaling and external V_{REFQ} at speeds faster than 200 MT/s, specified AC timings are not guaranteed. If not using the differential signaling, statements about those signal types can be ignored. ZQ calibration is optional for NV-DDR3 interface speeds faster than 533 MT/s but required to guarantee specified AC timings. If a host does not use ZQ calibration at speeds faster than 533 MT/s, specified AC timings are not guaranteed.

The NV-DDR3 interface bus modes are summarized below:

Table 4: NV-DDR3 Interface Mode Selection

Mode	CE#	CLE	ALE	RE# (RE_t)	RE_c[8]	DQS (DQS_t)	DQS_c[8]	DQ[7:0][1]	WE#	WP#	Notes
Standby	H	X	X	X	X	X	X	X	X	0V/V_{CCQ}	1, 2
Idle	L	L	L	H	L	H	L	X	H	X	6
Command input	L	H	L	H	L	H	L	input		H	3
Address input	L	L	H	H	L	X[4]	X	input		H	3
Data input	L	L	L	H	L			input	H	H	2, 3
Data output	L	L	L					output	H	X	2, 3, 5
Write protect	X	X	X	X	X	X	X	X	X	L	

Notes: 1. The current state of the device is data input, data output, or neither based on the commands issued.
2. There are two data input/output cycles from the rising edge of DQS/RE# to the next rising edge of DQS/RE#.
3. ODT may be enabled as part of the data input and data output cycles.
4. When ODT is enabled and anytime CE#, ALE, CLE, and DQS are LOW, additional current may result.
5. At the beginning of a data output burst, DQS shall be held HIGH for ^{t}DQSRH after RE# transitions LOW to begin data output. ^{t}DQSRH is only required if Matrix ODT is enabled
6. WE# is set HIGH during the Idle state.
7. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.
8. If RE_c and/or DQS_c are not enabled, these signals can be treated as a Don't Care.

Differential Signaling

An enabler for higher speed operation is differential signaling for the RE# and DQS signals. A complementary RE# and complementary DQS signal may be optionally used to create differential signal pairs (RE_t/RE_c and DQS_t/DQS_c). When using differential signaling, RE# is referred to as RE_t and DQS is referred to as DQS_t, that is, the "true" versions of the signals. Differential signaling may be used to improve signal integrity through enhanced noise immunity. Differential signaling shall only be enabled for use when the NV-DDR3 data interface is selected.

A device may support differential RE# and/or differential DQS signaling. The support for differential RE# and/or DQS is reported in the parameter page. Complementary RE# (that is, RE_c) and comple-

mentary DQS (that is, DQS_c) signals are individually configured/enabled. By default, differential signaling is disabled. The host may configure the device to use differential signaling using the NV-DDR3 Configuration feature address.

Differential signaling is not enabled by default. It is recommended that if differential signaling is used by a host system that is it enabled at the same time as the interface utilizing the differential signaling is enabled.

To begin using differential signaling, the host shall issue a SET FEATURES (EFh) command to the NV-DDR3 Configuration feature address to activate differential RE# and/or differential DQS signaling. The host shall then bring CE# high and wait until either ^{t}FEAT time has elapsed or the R/B# signal is back high, prior to issuing any command (including Read Status commands) to the device. The new configuration settings shall be ready to use after either the ^{t}FEAT time has elapsed or the R/B# signal is back high.

To change from differential signaling to single-ended signaling, the host shall configure the device using the NV-DDR3 Configuration feature address to disable differential signaling. The host shall then bring CE# high and wait until either ^{t}FEAT time has elapsed or the R/B# signal is back high, prior to issuing any command (including Read Status commands) to the device. The new configuration settings shall be ready to use after either the ^{t}FEAT time has elapsed or the R/B# signal is back high.

A RESET (FFh) command will not disable differential signaling. The RESET LUN (FAh) command has no effect on differential signaling.

Warmup Cycles

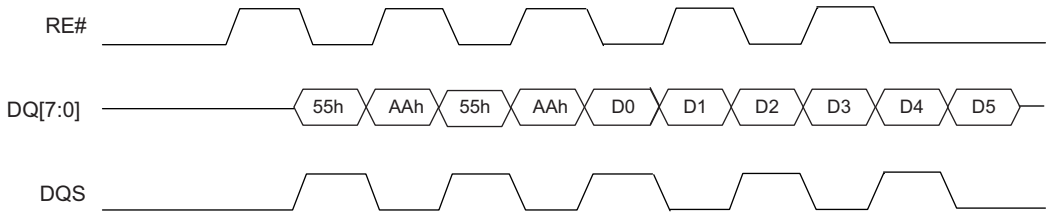
In order to support higher speed operation, warmup cycles for data output and data input may be provided. Warmup cycles shall only be enabled for use when the NV-DDR3 data interface is selected. For speeds greater than 800 MT/s, warmup cycles are required for both data input and output.

Warmup cycles for data output provides extra RE# and corresponding DQS transitions at the beginning of a data output burst. These extra RE#/DQS transitions do not have any data associated with them. The number of extra cycles is configured via the NV-DDR3 configuration feature address.

Warmup cycles for data input provides extra DQS transitions at the beginning of a data input burst. These extra DQS transitions do not have any data associated with them. The number of extra cycles is configured via the NV-DDR3 Configuration feature address. The number of cycles specified includes a full data input cycle (both rising and falling edge for DQS).

Warmup cycles are optional for both data output and data input, and if used, do not need to be configured to the same value. Warmup cycles apply to all commands. Warmup cycles are initiated at the start of each data burst when warmup cycles are enabled for that data transfer type. If the host pauses and then resumes a data transfer without exiting and re-entering the data burst, then the host shall not issue additional warmup cycles. Exiting and re-entering the data burst shall be performed by bringing ALE, CLE, or CE# HIGH without latching with WE#. In the case of not re-issuing warmup cycles, the host should take care to avoid signal integrity issues due to pausing the data transfer and resuming without warmup cycles.

Figure 15: Warmup Cycles for Data Output (2 Warmup Cycles)



Note: 1. The output warmup pattern on DQ[7:0] may be different on the actual device and for different operations.

Warmup Cycle Restrictions

For read operations to the NAND cache register if the host enables data output warmup cycles on a LUN through Feature Address 02h: NV-DDR3 configuration, subfeature P2 DQ[3:0] and the host exits the data output burst for the LUN after issuing at least 1 warmup cycle but prior to the toggling out of 2 bytes of data from the LUN, the host is required to issue a CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command prior to resuming the data output burst on that LUN.

For READ ID (90h) and during READ DQ TRAINING (62h) operations, if the host enables data output warmup cycles on a LUN through Feature Address 02h: NV-DDR3 configuration, subfeature P2 DQ[3:0], and the host exits the data output burst for the LUN after issuing at least 1 warmup cycle but prior to the toggling out of 2 bytes of data from the LUN, the host is required to re-issue the command again and restart the data output burst.

On-Die Termination

On-die termination (ODT) may be required at higher speeds depending on system topology. On-die termination applies to the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals. On-die termination is an optional capability that may be employed to meet higher speeds in particular topologies. On-die termination can improve signal quality by reducing signal reflection through internal termination resistance adjustment. If power needs to be optimized in a particular condition, then on-die termination may be disabled and the topology may be run at a slower timing mode.

On-die termination settings are configured during device initialization. The host may configure the ODT in a self-termination only configuration, or matrix termination which enables a combination of Target and non-Target termination to be specified.

For the more flexible matrix termination the host configures a matrix that defines the LUN(s) that terminate for a particular Volume. This matrix is configured using the ODT CONFIGURE (E2h) command. After the on-die termination matrix is defined, ODT is enabled and disabled based on the type of cycle (on for data input and output cycles, off for command, and address cycles). On-die termination applies for data input and output cycles for all command types, including both single data rate (SDR) and double data rate (DDR) transfers.

Volume addressing is required for use of non-Target on-die termination (ODT) functionality. See Configuration Operations for how to appoint Volume addresses. Once volume addresses have been appointed they can be selected with the VOLUME SELECT (E1h) command. For Target only termination, no ODT termination matrix is required.

The on-die termination configuration matrix and control mechanism utilize Volume addresses. Volume addressing is a required capability to utilize non-Target on-die termination.

The on-die termination settings are retained across RESET (FAh, FFh) commands, but are not retained across HARD RESET (FDh) commands for the target LUN.

When on-die termination is enabled via feature address, the default is Target termination. For non-Target termination or termination topologies that use multiple terminators, the Volume address mechanism shall be used and the on-die termination configuration matrix shall be specified using the ODT CONFIGURE (E2h) command. As part of the ODT CONFIGURE (E2h) command, R_{TT} settings may be specified on a per LUN basis with individual values for:

- RE#
- DQ[7:0] and DQS for data output
- DQ[7:0] and DQS for data input

On-die termination is enabled when ALE, CLE, and CE# transition from HIGH to LOW. On-die termination is disabled when ALE, CLE, or CE# transitions from LOW to HIGH.

Table 5: On-die Termination DC Electrical Characteristics without ZQ Calibration

Mode	Symbol	Min	Typ	Max	Units	Notes
R_{TT} effective impedance value for 50 ohm setting	$R_{TT1(EFF)}$	32.5	50	80	ohms	1
R_{TT} effective impedance value for 75 ohm setting	$R_{TT2(EFF)}$	48.5	75	120	ohms	1
R_{TT} effective impedance value for 150 ohm setting	$R_{TT4(EFF)}$	97.5	150	240	ohms	1
Deviation of VM with respect to $V_{CCQ}/2$	?VM	–7	–	7	Percent	2

Notes: 1. $R_{TT1\ (EFF)}$, $R_{TT2\ (EFF)}$ and $R_{TT4\ (EFF)}$ are determined by separately applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to the signal being tested, and then measuring current $I(V_{IH[AC]})$ and $I(V_{IL[AC]})$, respectively. $R_{TT(EFF)} = (V_{IH[AC]} - V_{IL[AC]})/(I(V_{IH[AC]}) - I(V_{IL[AC]})$
2. Measure voltage (VM) at the tested signal with no load. ?VM = [(2 x VM)/V_{CCQ} - 1] x 100.

Table 6: On-die Termination DC Electrical Characteristics with ZQ Calibration

Mode	Symbol	Min	Typ	Max	Units	Notes
R_{TT} effective impedance value	$R_{TT(EFF)}$	See following table ($R_{TT(EFF)}$ Impedance Values with ZQ Calibration)				1
Deviation of VM with respect to $V_{CCQ}/2$	?VM	–7	–	7	Percent	2

Notes: 1. $R_{TT\ (EFF)}$ is determined by separately applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to the signal being tested, and then measuring current $I(V_{IH[AC]})$ and $I(V_{IL[AC]})$, respectively. $R_{TT(EFF)} = (V_{IH[AC]} - V_{IL[AC]})/(I(V_{IH[AC]}) - I(V_{IL[AC]})$
2. Measure voltage (VM) at the tested signal with no load. ?VM = [(2 x VM)/V_{CCQ} - 1] x 100.

Table 7: $R_{TT(EFF)}$ Impedance Values with ZQ Calibration

R_{TT}	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
50 ohms	Rpd [4]	V_{CCQ} × 0.2	0.57	1	1.15	RZQ/3
		V_{CCQ} × 0.5	0.85	1	1.15	RZQ/3
		V_{CCQ} × 0.8	0.85	1	1.47	RZQ/3
	Rpu [4]	V_{CCQ} × 0.2	0.85	1	1.47	RZQ/3
		V_{CCQ} × 0.5	0.85	1	1.15	RZQ/3
		V_{CCQ} × 0.8	0.57	1	1.15	RZQ/3
50 ohms [5]		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.85	1	1.67	RZQ/6

Table 7: $R_{TT(EFF)}$ Impedance Values with ZQ Calibration

R_{TT}	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
75 ohms	Rpd [4]	V_{CCQ} × 0.2	0.57	1	1.15	RZQ/2
		V_{CCQ} × 0.5	0.85	1	1.15	RZQ/2
		V_{CCQ} × 0.8	0.85	1	1.47	RZQ/2
	Rpu [4]	V_{CCQ} × 0.2	0.85	1	1.47	RZQ/2
		V_{CCQ} × 0.5	0.85	1	1.15	RZQ/2
		V_{CCQ} × 0.8	0.57	1	1.15	RZQ/2
75 ohms [5]		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.85	1	1.67	RZQ/4
150 ohms	Rpd [4]	V_{CCQ} × 0.2	0.57	1	1.15	RZQ/1
		V_{CCQ} × 0.5	0.85	1	1.15	RZQ/1
		V_{CCQ} × 0.8	0.85	1	1.47	RZQ/1
	Rpu [4]	V_{CCQ} × 0.2	0.85	1	1.47	RZQ/1
		V_{CCQ} × 0.5	0.85	1	1.15	RZQ/1
		V_{CCQ} × 0.8	0.57	1	1.15	RZQ/1
150 ohms [5]		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.85	1	1.67	RZQ/2

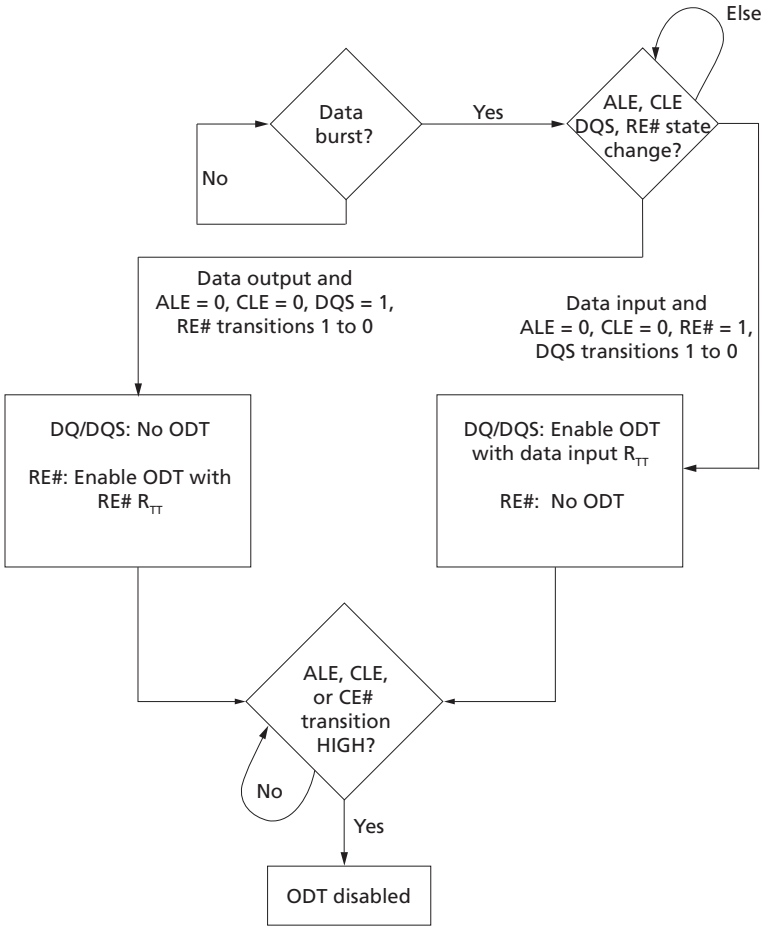
Notes: 1. Tolerance limits assume R_{ZQ} of 300 ohms ±1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.
3. The minimum values are derated by 6% when the device operates between –40°C and 0°C.
4. Rpd and Rpu are not specification requirements but may be used as design guidelines.
5. The Rtt Maximum, Nominal and Minimum specifications for a V_{OUT} to V_{SSQ} between $V_{IL(AC)}$ to $V_{IH(AC)}$, are specification requirements.

Self-Termination On-Die Termination

When self-termination is enabled, the LUN that is executing the command provides on-die termination. Figure 16 defines the self-termination only ODT enable and disable requirements for the LUN that is executing the command when ODT is selected for use via SET FEATURES (EFh) command. If the ODT CONFIGURE (E2h) command is issued to a LUN on a Target, then the ODT mechanism used for that Target changes to matrix termination.

Self-termination is applied to DQS and DQ[7:0] signals during data input operations and RE# during data output operations.

Figure 16: Self-Termination Only ODT Behavioral Flow



Matrix Termination

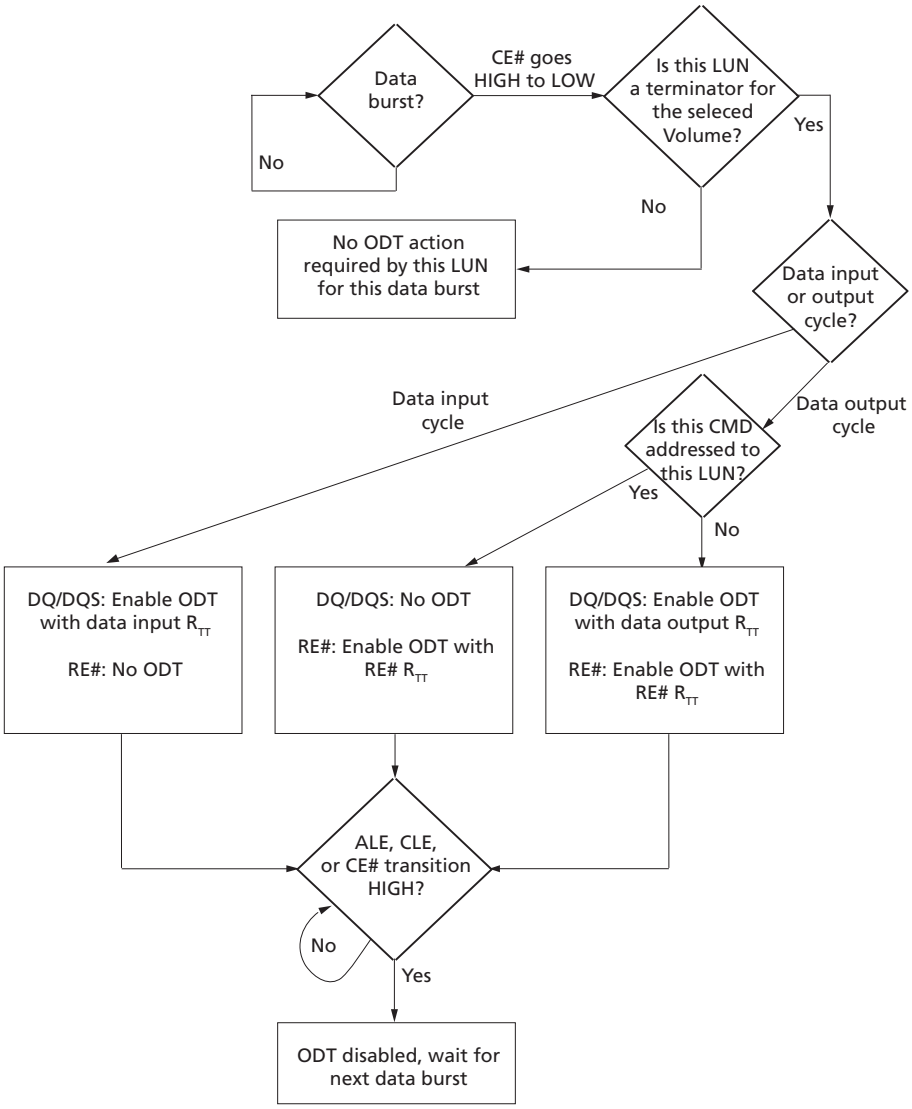
A LUN that is configured to act as a terminator using the configuration matrix (that is specified with the ODT CONFIGURE (E2h) command) may be located on the selected Volume as the Volume it is terminating for (Target termination) or a unselected Volume (non-Target termination). Based on the ODT configuration and the Volume a command is addressed to, LUNs enter different states which determine their ODT behavior; those states are listed in the LUN state for Matrix Termination Table .

Table 8: LUN state for Matrix Termination

LUN is on Selected Volume?	Terminator for Selected Volume?	LUN State	ODT Actions Defined
Yes	N/A	Selected	Figure 17
No	Yes	Sniff	Figure 18
No	No	Deselected	No ODT actions

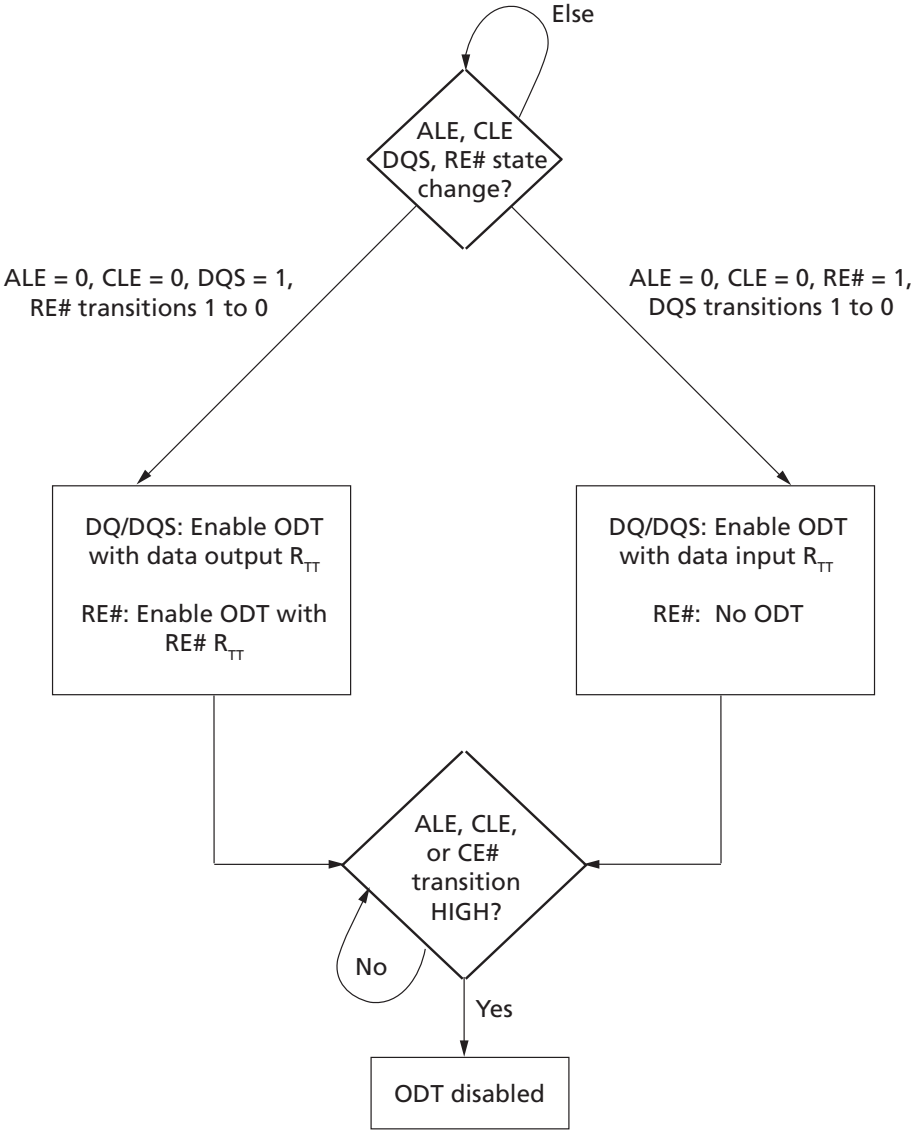
The LUN that a command is addressed to for execution may provide termination. Other LUNs on the selected Volume that are not responsible for execution of the command may also provide termination. Figure 17 defines the ODT actions required for LUNs of each of these types on the selected Volume. LUNs on the selected Volume remain in an active state, and thus are aware of state information like whether there is a data burst currently and the type of cycle; These LUNs do not rely only on ALE, CLE, DQS, and RE# signals.

Figure 17: ODT Actions for LUNs on Selected Volume



The ODT configuration matrix also offers the flexibility of having LUNs on an unselected Volume provide termination for the selected Volume. When a LUN is placed in the Sniff state, it checks the ALE, CLE, DQS and RE# signals to determine when to enable or disable ODT. Figure 18 defines the ODT actions for LUNs in the Sniff state on an unselected Volume.

Figure 18: ODT Actions for LUNs in Sniff State on Unselected Volume



Matrix Termination Examples

This section describes two examples of on-die termination configurations using matrix termination. In both examples, there are two Volumes appointed. Each Volume consists of four LUNs, referred to as H0N*n*-LUN0 through H0N*n*-LUN3. The following Volume addresses were appointed at initialization.

Table 9: Volume Appointment for Matrix Termination Example

Volume	Appointed Volume Address
H0N0	0
H0N1	1

For optimal signal integrity and power consumption, the host may configure termination in a variety of ways. The host may configure a LUN to self terminate, perform non-Target termination for another Volume, or not perform any termination function. Using matrix termination, the termination R_{TT}

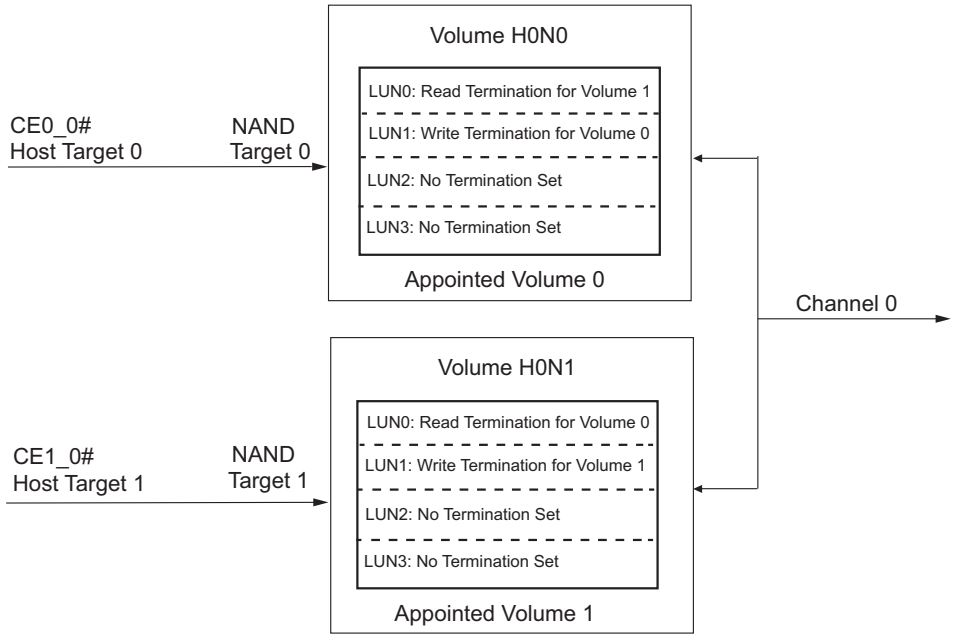
values may be set differently for each LUN configured as a terminator, including the ability to specify different settings for data output operation and data input operation. The first example shows that a controller may configure the ODT matrix to perform stronger non-Target ODT for data output operations and weaker Target ODT for data input operations.

Table 10: Non-Target ODT for Data Output, Target ODT for Data Input Settings Configuration Example

	Input values for ODT CONFIGURE (E2h)				Notes
LUN	Byte M0	Byte M1	Byte R_{TT1}	Byte R_{TT2}	
H0N0-LUN0	02h	00h	40h	03h	Terminates for Volume 1 (non-Target) for data output with an R_{TT} value of 50 ohms for DQ[7:0]/DQS and 75 ohms for RE#
H0N0-LUN1	01h	00h	01h	00h	Terminates for Volume 0 (Target) for data input with an R_{TT} value of 150 ohms for DQ[7:0]/DQS
H0N0-LUN2	00h	00h	00h	00h	Does not act as terminator
H0N0-LUN3	00h	00h	00h	00h	Does not act as terminator
H0N1-LUN0	01h	00h	40h	03h	Terminates for Volume 0 (non-Target) for data output with an R_{TT} value of 50 ohms for DQ[7:0]/DQS and 75 ohms for RE#
H0N1-LUN1	02h	00h	01h	00h	Terminates for Volume 1 (Target) for data input with an R_{TT} value of 150 ohms for DQ[7:0]/DQS
H0N1-LUN2	00h	00h	00h	00h	Does not act as terminator
H0N1-LUN3	00h	00h	00h	00h	Does not act as terminator

Notes: 1. See ODT CONFIGURE (E2h) for details on input values for ODT CONFIGURE (E2h).

Figure 19: Non-Target ODT for Data Output, Target ODT for Data Input Configuration Example

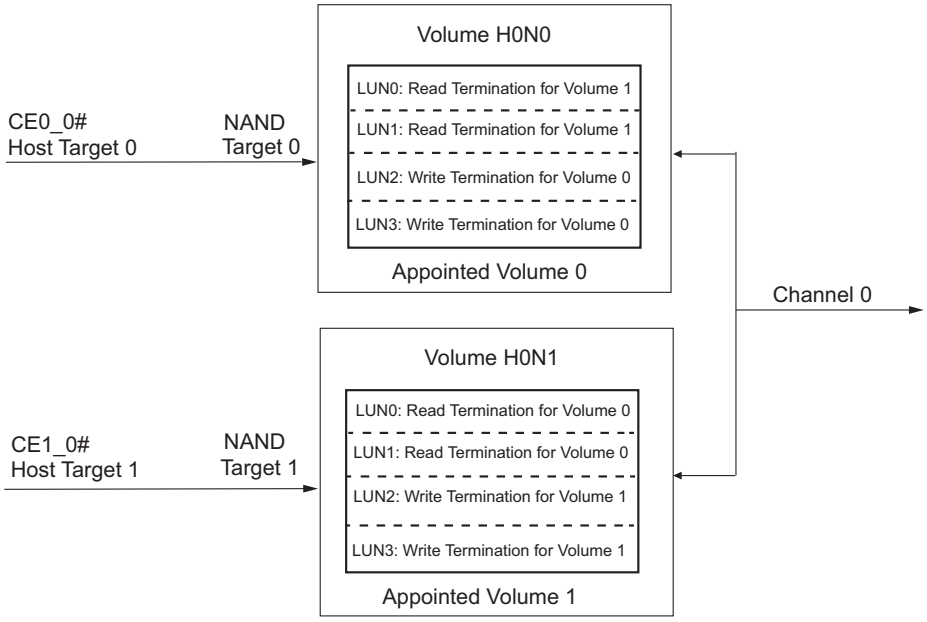


The second example uses parallel non-Target termination to achieve a stronger effective R_{TT} value for both data output and data input operations. For data output, two 50 ohm terminators are used in parallel to achieve an effective 25 ohms non-Target termination value. For data input, two 150-ohm terminators are used in parallel to achieve an effective 75 ohms non-Target termination value. This type of ODT matrix allows for stronger termination than may be available through a single device. It also allows for intermediate R_{TT} values with the use of different R_{TT} values for parallel LUNs. For example, if one terminator was configured for 50 ohms and another terminator was configured for 150 ohms for the same Volume then an effective R_{TT} value of 37.5 ohms is achieved. In this example, parallel termination is used for data input and data output for DQ[7:0]/DQS, however, RE# is not terminated.

Table 11: Parallel Non-Target ODT Settings Configuration Example

	Input Values for ODT CONFIGURE (E2h)				Notes
LUN	Byte M0	Byte M1	Byte R_{TT1}	Byte R_{TT2}	
H0N0-LUN0	02h	00h	40h	00h	Terminates for Volume 1 (non-Target) for data output with an R_{TT} value of 50 ohms for DQ[7:0]/DQS
H0N0-LUN1	02h	00h	40h	00h	Terminates for Volume 1 (non-Target) for data output with an R_{TT} value of 50 ohms for DQ[7:0]/DQS
H0N0-LUN2	01h	00h	01h	00h	Terminates for Volume 0 (Target) for data input with an R_{TT} value of 150 ohms for DQ[7:0]/DQS
H0N0-LUN3	01h	00h	01h	00h	Terminates for Volume 0 (Target) for data input with an R_{TT} value of 150 ohms for DQ[7:0]/DQS
H0N1-LUN0	01h	00h	40h	00h	Terminates for Volume 0 (non-Target) for data output with an R_{TT} value of 50 ohms for DQ[7:0]/DQS
H0N1-LUN1	01h	00h	40h	00h	Terminates for Volume 0 (non-Target) for data output with an R_{TT} value of 50 ohms for DQ[7:0]/DQS
H0N1-LUN2	02h	00h	01h	00h	Terminates for Volume 1 (Target) for data input with an R_{TT} value of 150 ohms for DQ[7:0]/DQS
H0N1-LUN3	02h	00h	01h	00h	Terminates for Volume 1 (Target) for data input with an R_{TT} value of 150 ohms for DQ[7:0]/DQS

Figure 20: Parallel Non-Target ODT Configuration Example



NV-DDR3 Standby

Prior to disabling a target, the target's bus must be idle. A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations.

NV-DDR3 Idle

A target's bus is idle when CE# is LOW, ALE is LOW, CLE is LOW, RE# is HIGH, and DQS is HIGH and no internal LUN operations are ongoing or data being inputted or outputted from the target. DQS is driven HIGH to prevent the device from enabling ODT. If ODT is disabled, then DQS is a Don't Care during Idle states.

During the bus idle mode, all signals are enabled. No commands, addresses, or data are latched into the target; no data is output.

NV-DDR3 Pausing/Exiting/Interrupting Data Input/Output

Pausing data input or data output may be done by placing the bus in an Idle state. The pausing of data output may also be done in the middle of a data output burst by pausing RE# and holding the signal(s) static HIGH or LOW until the data burst is resumed. The pausing of data input may also be done in the middle of a data input burst by pausing DQS and holding the signal(s) static HIGH or LOW until the data burst is resumed. WE# shall be held HIGH during data input and output burst pause time. ODT (if enabled) stays ON the entire pause time and warmup cycles (if enabled) are not re-issued when re-starting a data burst from pause.

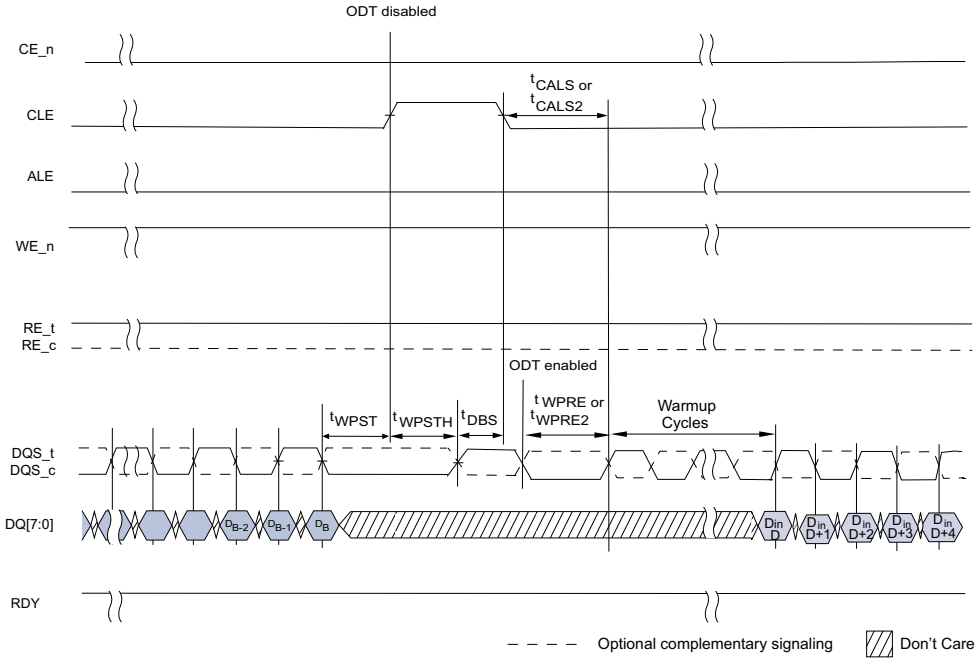
Pausing in the middle of a data input or data output burst is only allowed up to the 800 MT/s data rate. Above 800 MT/s, pausing in the middle of a data input or data output burst is not allowed, and if the data burst is interrupted, the host is required to exit first the data burst prior to resuming it.

A data burst is exited when either ALE or CLE or CE# is toggled to a 1. After a data burst has been exited, if warmup cycles are enabled, then warmup cycles are required when restarting the data burst. After a data burst has been exited, ODT also may be disabled, however if needed to meet the signal integrity needs of the system, ODT must be re-enabled prior to restarting the data burst. If the host wishes to end the data burst, after exiting the data burst, a new command is issued.

A data burst is interrupted when it is either paused or exited.

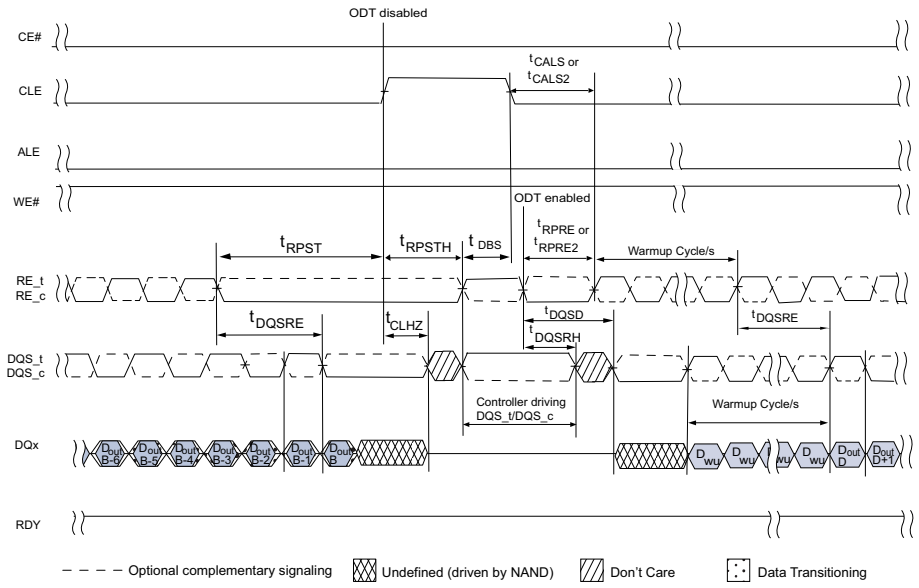
The figure below is an example of exiting a data input burst with a CLE = 1 and resuming the data input burst with a CLE = 0. Warmup cycles if enabled are required to be issued when the data input burst is resumed.

Figure 21: Data Input Burst Exit with CLE HIGH and Resume with CLE LOW



The figure below is an example of exiting a data output burst with a CLE = 1 and resuming the data output burst with a CLE = 0. Warmup cycles if enabled are required to be issued when the data output burst is resumed.

Figure 22: Data Output Burst Exit with CLE HIGH and Resume with CLE LOW



Interrupting a data input or data output sequence by toggling CE# HIGH is also allowed, but subject to the requirements in the Data Input Sequence Interruption and Resume requirements Table and the Data Output Sequence Interruption and Resume Requirements Table if the CE# HIGH pulse interruption is >1µs in duration.

Table 12: Data Input Sequence Interruption and Resume Requirements if Data Input Sequence is Interrupted by a CE# HIGH Pulse >1µs Duration

Command Sequence	Command Description	Timing of CE# HIGH pulse >1µs interruption	Requirement for Proper Data Input for the Interrupted Command Sequence
EFh-address-^{t}ADL-data input burst	Set Feature	During ^{t}ADL time or data input burst	CE# HIGH pulse >1µs is not allowed during ^{t}ADL time or data input burst.
D5h-address-^{t}ADL-data input burst	Set Feature by LUN		
E2h-address-^{t}ADL-data input burst	ODT Configure		
85h-2 address-^{t}CCS-data input burst	Change Write Column	During ^{t}CCS time	Issue an 11h command prior to CE# HIGH pulse >1µs to exit the data input burst. To start/resume the data input burst which has been exited with an 11h command, a CHANGE ROW ADDRESS (85h-6 address) shall be issued. Note that for the CHANGE WRITE COLUMN sequence (85h-2 address-^{t}CCS-data input burst) interrupted with a CE# HIGH pulse >1µs, a CHANGE ROW ADDRESS (85h-6 address-^{t}CCS-data input burst) is required to resume the data input burst.
		During data input burst	
85h-6 address-^{t}CCS-data input burst	Change Row Address	During ^{t}CCS time	
		During data input burst	

Table 12: Data Input Sequence Interruption and Resume Requirements if Data Input Sequence is Interrupted by a CE# HIGH Pulse >1µs Duration

Command Sequence	Command Description	Timing of CE# HIGH pulse >1µs interruption	Requirement for Proper Data Input for the Interrupted Command Sequence
85h-6 address-^{t}CCS-data input burst-10h/15h	Change Row Address with 10h/15h command	After data input burst but prior to 10h/15h command	Host shall either: 1) Issue the 10h/15h command prior to CE# HIGH pulse >1µs to first end the data input burst, or 2) issue an 11h command prior to CE# HIGH pulse >1µs, after CE# goes back low issue a CHANGE ROW ADDRESS (85h-6address)-no data input cycles-10h/15h sequence to end the data input burst.
80h-address-^{t}ADL-data input burst-10h/15h/11h	Program Page/Program Page Cache/Program Page Multi-plane	During ^{t}ADL time	Issue an 11h command prior to CE# HIGH pulse >1µs to exit the data input burst. To start/resume data input burst which has been exited with an 11h command, a CHANGE ROW ADDRESS (85h-6 address) shall be issued.
80h-address-^{t}ADL-data input burst-10h/15h	Program Page/Program Page Cache	During data input burst	
		After data input burst but prior to 10h/15 command	Host shall either: 1) Issue the 10h/15h command prior to CE# HIGH pulse >1µs to first end the data input burst, or 2) issue an 11h command prior to CE# HIGH pulse >1µs, after CE# goes back low issue a CHANGE ROW ADDRESS (85h-6address)-no data input cycles-10h/15h sequence to end the data input burst.
85h-6 address-^{t}CCS-data input burst-10h	Copyback Program	During ^{t}CCS time	Issue an 11h command prior to CE# HIGH pulse >1µs to exit the data input burst. To start/resume data input burst which has been exited with an 11h command, a CHANGE ROW ADDRESS (85h-6 address) shall be issued.
		During data input burst	
		After data input burst but prior to 10h	Host shall either: 1) Issue the 10h command prior to CE# HIGH pulse >1µs to first end the data input burst, or 2) issue an 11h command prior to CE# HIGH pulse >1µs, after CE# goes back low issue a CHANGE ROW ADDRESS (85h-6address)-no data input cycles-10h sequence to end the data input burst.

Table 12: Data Input Sequence Interruption and Resume Requirements if Data Input Sequence is Interrupted by a CE# HIGH Pulse >1µs Duration

Command Sequence	Command Description	Timing of CE# HIGH pulse >1µs interruption	Requirement for Proper Data Input for the Interrupted Command Sequence
80h-address-^{t}ADL-data input burst-10h	Program OTP Page/Protect OTP Area	During ^{t}ADL time	Issue an 11h command prior to CE# HIGH pulse >1µs to exit the data input burst. To start/resume data input burst which has been exited with an 11h command, a CHANGE ROW ADDRESS (85h-6 address) shall be issued.
		During data input burst	
		After data input burst but prior to 10h	Host shall either: 1) Issue the 10h command prior to CE# HIGH pulse >1µs to first end the data input burst, or 2) issue an 11h command prior to CE# HIGH pulse >1µs, after CE# goes back low issue a CHANGE ROW ADDRESS (85h-6address)-no data input cycles-10h sequence to end the data input burst.
63h-LUN address-^{t}ADL-data input burst	Write Training Tx	During ^{t}ADL	CE# HIGH pulse >1µs is not allowed during ^{t}ADL and the data input burst.
		During data input burst	

Table 13: Data Output Sequence Interruption and Resume Requirements if Data Output Sequence is Interrupted by a CE# HIGH Pulse >1µs Duration

Command Sequence	Command Description	Timing of CE# HIGH pulse >1µs interruption	Requirement for Proper Data Output for the Interrupted Command Sequence
00h-20h	IWL Read	After 20h command, during or after ^{t}RSNAP	After ^{t}RSNAP has completed, issue a CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) prior to starting/resuming data output burst. Use of CHANGE READ COLUMN (05h-E0h) with an IWL Read is prohibited.
00h-30h	Read Page	After 30h command, during or after ^{t}R	After ^{t}R/^{t}RCBSY1/^{t}RCBSY2/^{t}R_SBSBR has completed, issue a CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) prior to starting/resuming data output burst.
31h	Read Page Cache Sequential	After 31h command, during or after ^{t}RCBSY1 or ^{t}RCBSY2	
00h-31h	Read Page Cache Random	After 31h command, during or after ^{t}RCBSY1 or ^{t}RCBSY2	
3Fh	Read Page Last	After 3Fh command, during or after ^{t}RCBSY1 or ^{t}RCBSY2	
00h-35h	Copyback Read	After 35h command, during or after ^{t}R	
00h-34h	SBSBR Read	After 34h command, during or after ^{t}R_SBSBR	
05h-E0h	Change Read Column	After E0h command, prior to or during data output burst	Re-issue CHANGE READ COLUMN(05h-E0h) to start/resume data output burst.

Table 13: Data Output Sequence Interruption and Resume Requirements if Data Output Sequence is Interrupted by a CE# HIGH Pulse >1µs Duration

Command Sequence	Command Description	Timing of CE# HIGH pulse >1µs interruption	Requirement for Proper Data Output for the Interrupted Command Sequence
06h-E0h	Change Read Column Enhanced	After E0h command, prior to or during data output burst	Re-issue CHANGE READ COLUMN ENHANCED (06h-E0h) to start/resume data output burst.
00h-05h-E0h			Re-issue CHANGE READ COLUMN ENHANCED (00h-05h-E0h) to start/resume data output burst.
ECh-00h(address) ECh-40h (address)	Read Parameter Page	After 00h or 40h address cycle, prior to or during data output burst	After ^{t}R has completed, issue a CHANGE READ COLUMN (05h-E0h) prior to starting/resuming data output burst. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command is prohibited during READ PARAMETER PAGE mode.
90h-00h/20h/40h (address)	Read ID	After 00h/20h/40h address cycling, prior to or during data output burst	Re-issue 90h-00h/20h/40h(address) to restart Read ID sequence.
EDh-address	Read Unique ID	After address cycle, prior to or during data output burst	After ^{t}R has completed, issue a CHANGE READ COLUMN (05h-E0h) prior to starting/resuming data output burst. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command is prohibited during READ UNIQUE ID mode.
00h-30h	Read OTP	After 30h command, during or after ^{t}R	After ^{t}R has completed, issue a CHANGE READ COLUMN (05h-E0h) prior to starting/resuming data output burst. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command is prohibited during READ OTP mode.
70h	Read Status	After 70h command but prior to data output	Proceed to status output, no need to re-issue 70h to restart Read Status sequence
78h-address	Read Status Enhanced	After 78h-address sequence but prior to data output	Proceed to status output, no need to re-issue 78h-address to restart Read Status Enhanced sequence.
71h-address	Fixed Address Read Status Enhanced	After 71h-address sequence but prior to data output	Proceed to status output, no need to re-issue 71h-address to restart Fixed Address Read Status Enhanced sequence.
79h-address	Extended Status Register Read	After 79h-address sequence but prior to data output	Proceed to status output, no need to re-issue 79h-address to restart Extended Status Register Read sequence.
EEh-address	Get Features	After EEh-address sequence but prior to data output burst	Proceed to feature data output, no need to re-issue EEh-address to restart Get Feature sequence.
D4h-address	Get Features by LUN	After D4h-address sequence but prior to data output burst	Proceed to feature data output, no need to re-issue D4h-address to restart Get Features by LUN sequence.
62h-address	Read Training	After 62h-address sequence but prior to data output burst, during ^{t}WHRT time	Re-issue 62h-address

Table 13: Data Output Sequence Interruption and Resume Requirements if Data Output Sequence is Interrupted by a CE# HIGH Pulse >1µs Duration

Command Sequence	Command Description	Timing of CE# HIGH pulse >1µs interruption	Requirement for Proper Data Output for the Interrupted Command Sequence
64h-address	Write Training Tx Read Back	After 64h-address sequence but prior to data output burst, during ^{t}WHRT time	Re-issue 64h-address
00h-05h-E0h During DCC Training	DCC Training	After E0h but prior to any RE toggles for DCC training during ^{t}WHRT time	Proceed to RE toggles, no need to re-issue 00h-05h-E0h

Figure 23: Data Input Burst Interruption and Resume with CE# HIGH >1µs

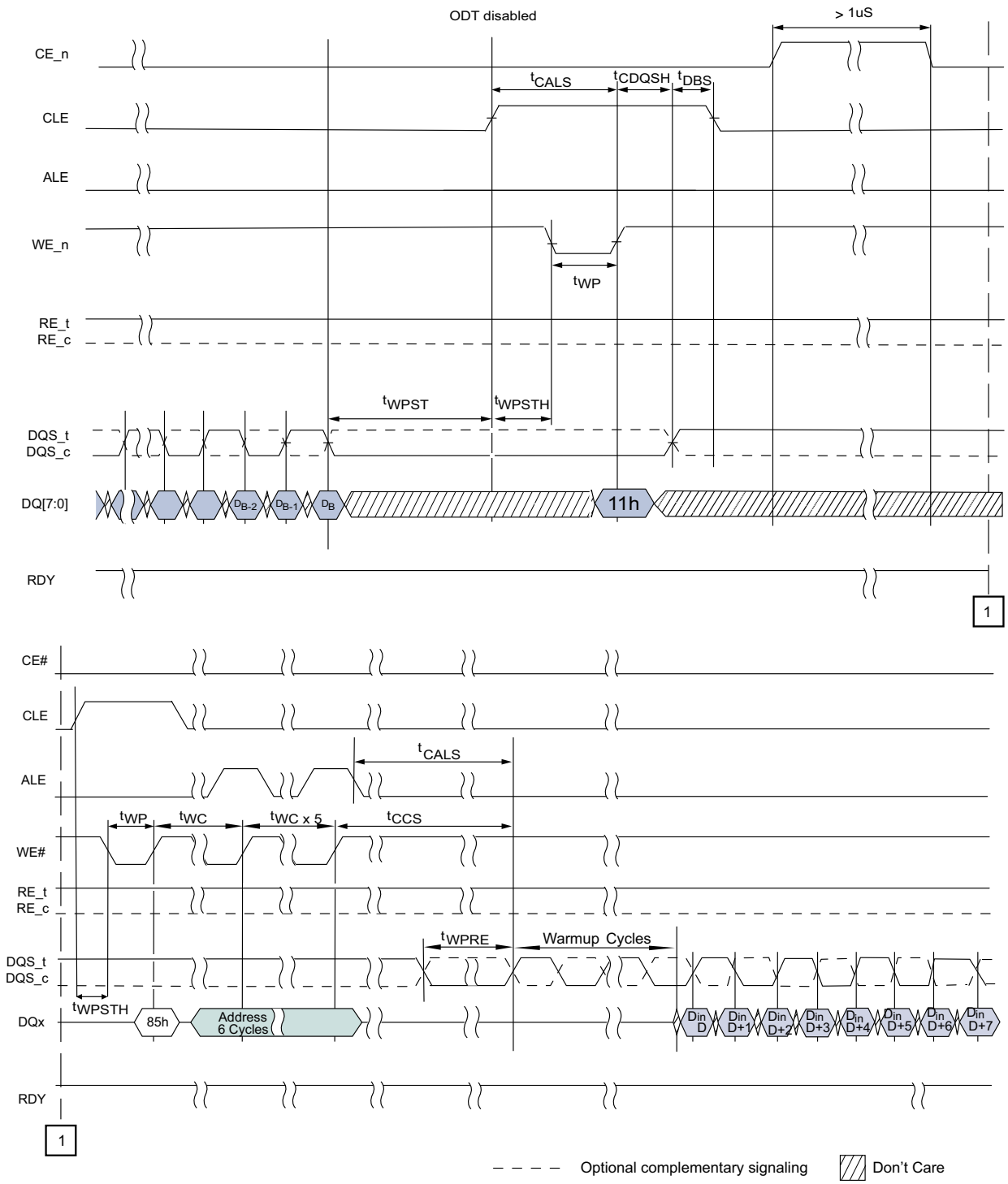
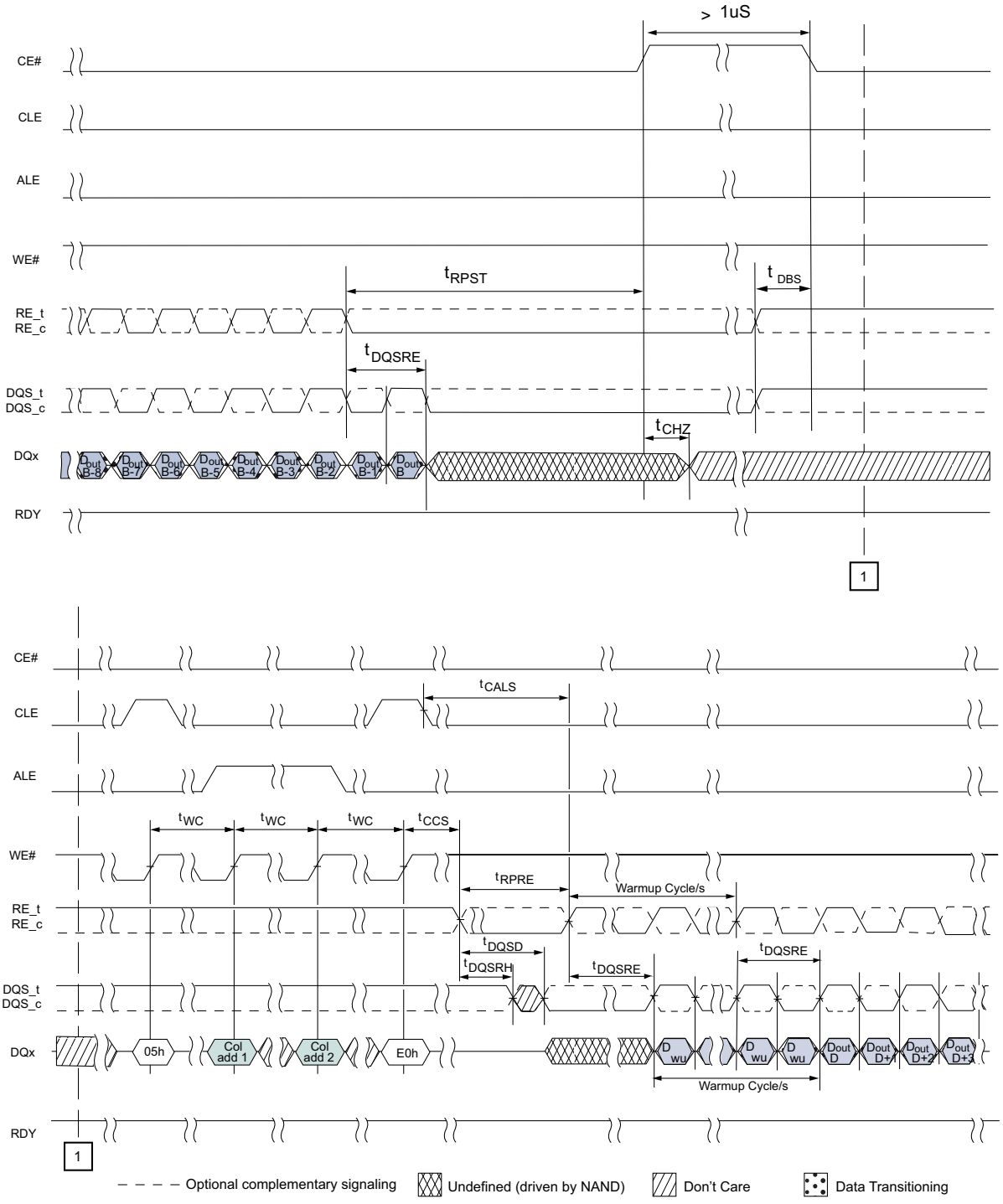


Figure 24: Data Output Burst Interruption and Resume with CE# HIGH >1µs

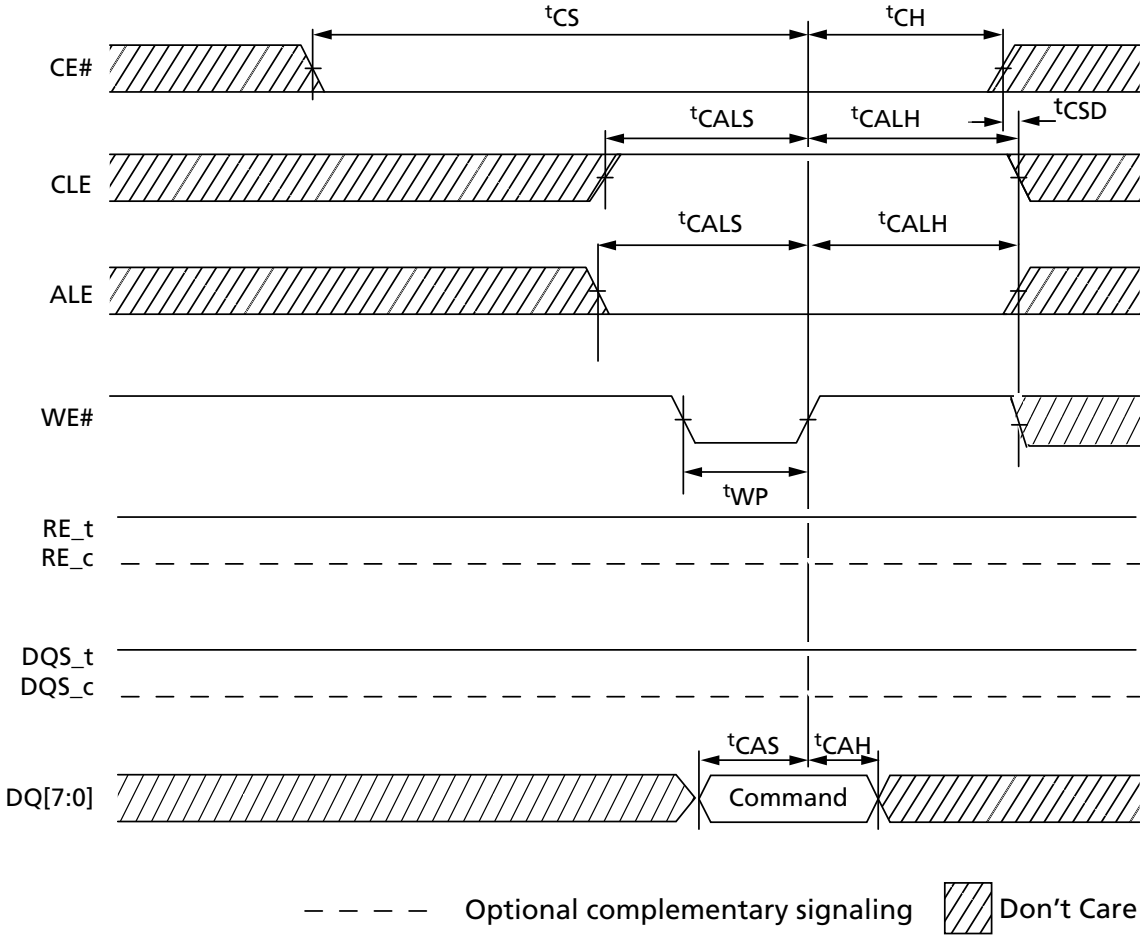


NV-DDR3 Commands

A command is written from DQ[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, such as READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs), even when they are busy.

Figure 25: NV-DDR3 Command Cycle



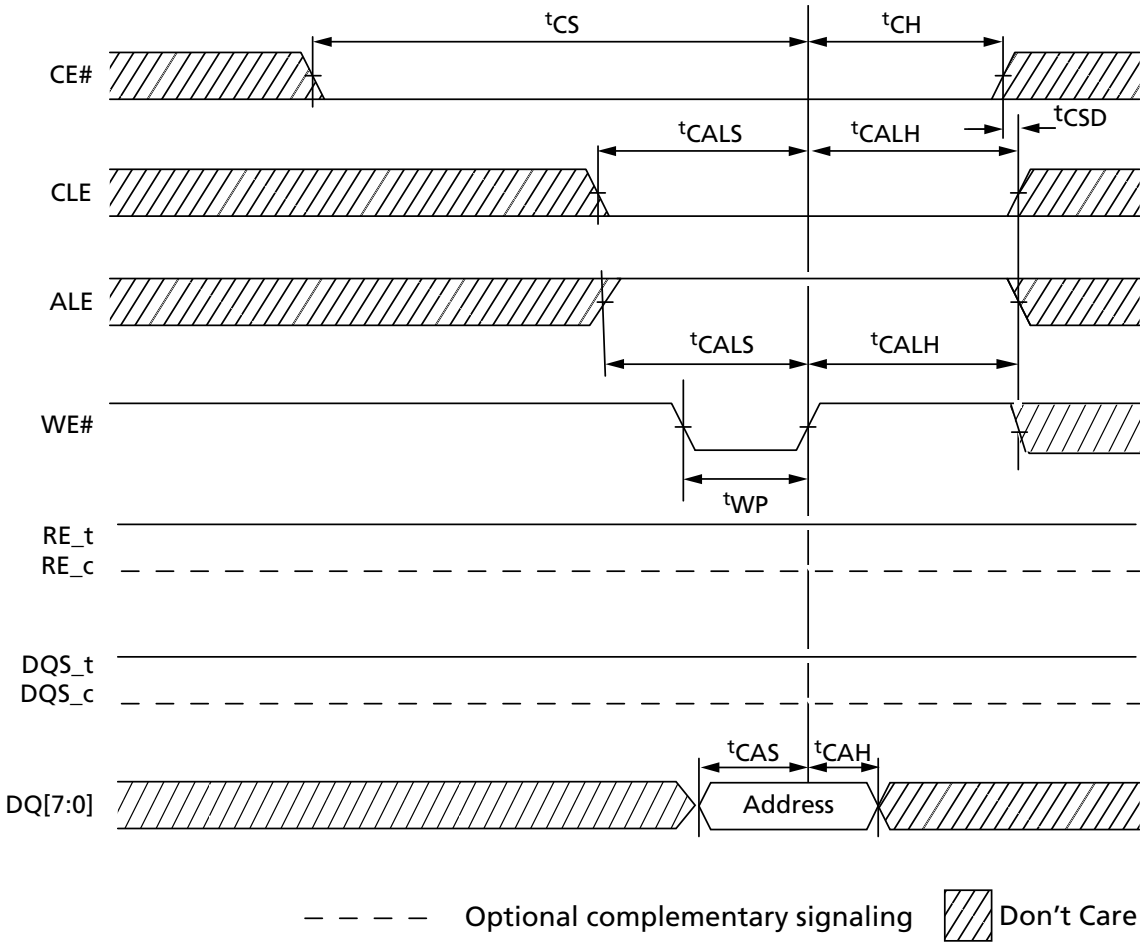
NV-DDR3 Addresses

A NV-DDR3 address is written from DQ[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits not part of the address space must be LOW (see Device and Array Organization). The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses such as address cycles that follow the READ STATUS ENHANCED (78h) command, are accepted by die (LUNs), even when they are busy.

Figure 26: NV-DDR3 Addresses Cycle



NV-DDR3 Data Input

To enter the NV-DDR3 data input mode, the following conditions must be met:

- CE# is LOW
- ALE and CLE are LOW
- RE# is HIGH
- tWPRE is met
- DQS is LOW

Upon entering the NV-DDR3 data input mode after tWPRE, data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when CE# is LOW, RE# is HIGH, and ALE and CLE are LOW.

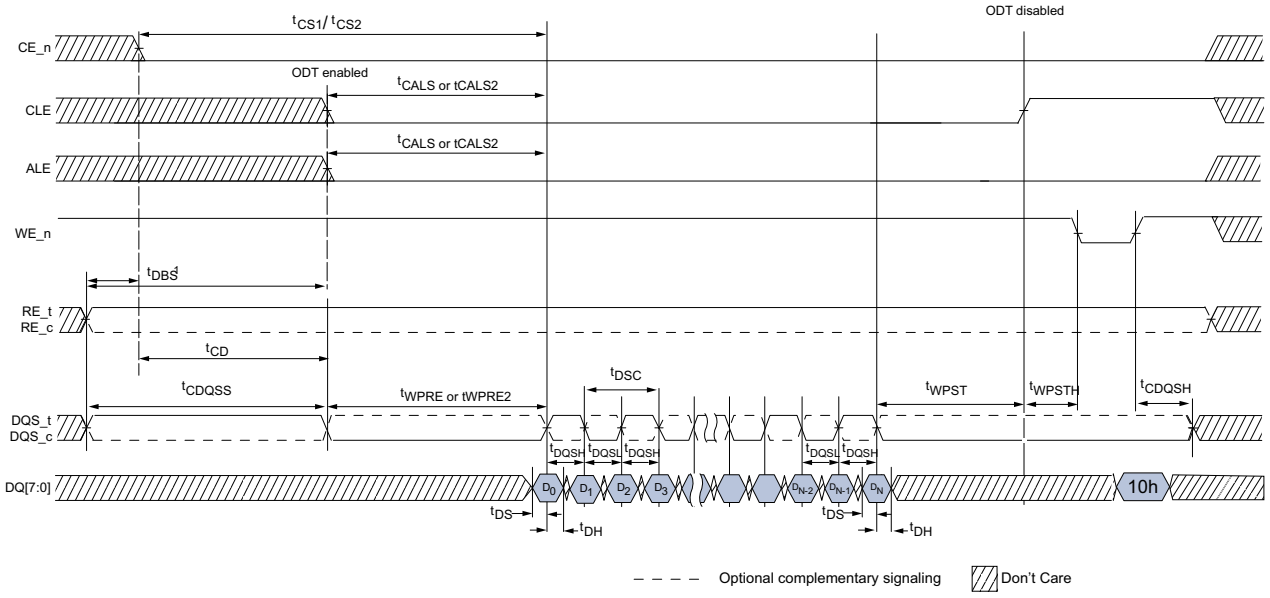
To exit NV-DDR3 data input mode, the following conditions must be met:

- CE# is LOW
- ALE and CLE are LOW
- RE# is HIGH
- The final two data bytes of the data input sequence are written to DQ[7:0] to the cache register on the rising and falling edges of DQS after the last cycle in the data input sequence
- DQS is held LOW for tWPST (after the final falling edge of DQS)

Following tWPST, CE#, CLE, or ALE should be brought HIGH to exit the data burst.

Data input is ignored by die (LUNs) that are not selected or are busy.

Figure 27: NV-DDR3 Data Input Cycles



Notes: 1. ODT may not be required to be used for data input. If ODT is selected for use via SET FEATURES (EFh), then ODT is enabled and disabled during the points indicated.
2. ODT is disabled on the rising edge of CE#, CLE, or ALE whichever occurs first.

NV-DDR3 Data Output

Data can be output from a die (LUN) if it is ready. Data output is supported following a READ operation from the NAND Flash array.

To enter the NV-DDR3 data output mode, the following conditions must be met:

- CE# is LOW
- The host has released the DQ[7:0] bus and DQS
- ALE and CLE are LOW
- tRPRE is met

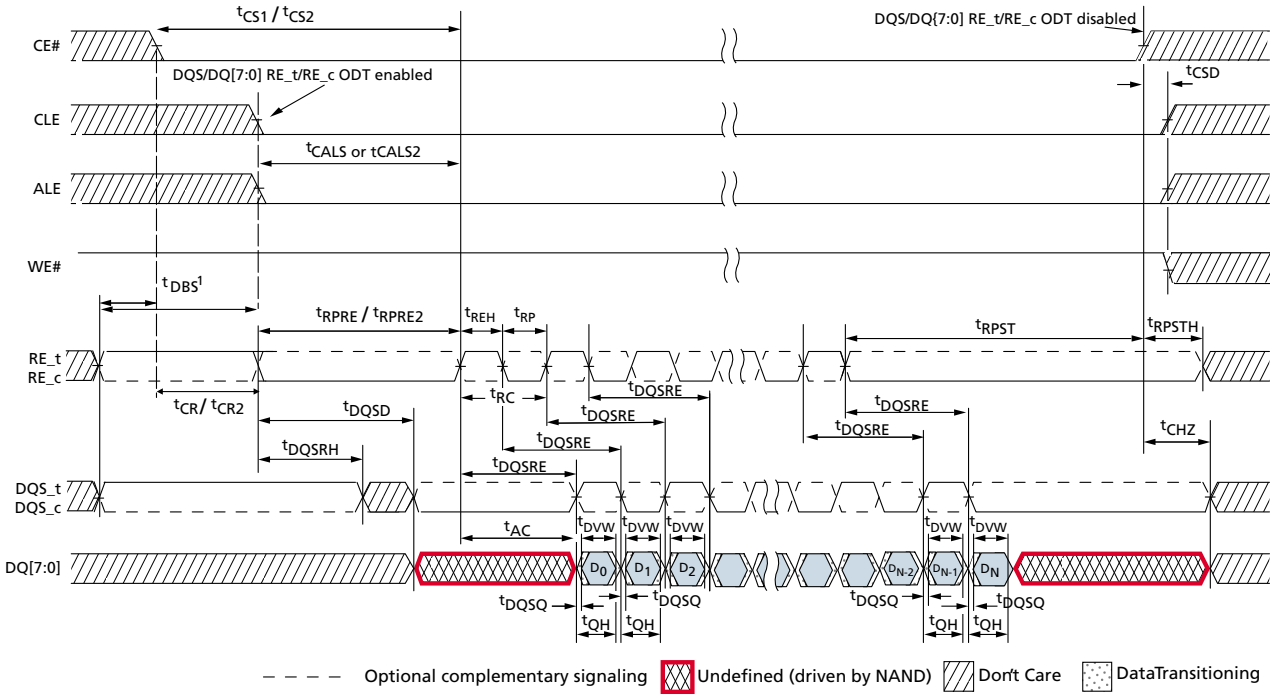
Upon entering the NV-DDR3 data output mode, DQS will toggle HIGH and LOW with a delay of tDQSRE from the respective rising and falling edges of RE#. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than tAC.

The final two data bytes are output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur tDQSRE after the last cycle in the data output sequence. The host must hold RE# for tRPST after the last RE# falling edge for data output.

Following tRPST, CE#, CLE, or ALE should be brought HIGH to exit the data burst.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

Figure 28: NV-DDR3 Data Output Cycles



Notes: 1. ODT may not be required to be used for data output. If ODT is selected for use via SET FEATURES (EFh), then ODT is enabled and disabled during the points indicated.
2. tDQSRH is only required if Matrix ODT is enabled.
3. ODT is disabled on the rising edge of CE#, CLE, or ALE whichever occurs first.

Write Protect

The write protect# (WP#) signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled.

It is recommended that the host drive WP# LOW during power-on until V_{CC} and V_{CCQ} are stable to prevent inadvertent PROGRAM and ERASE operations (see Device Initialization section for additional details).

WP# must be transitioned only when the target is not busy and prior to beginning a command sequence. After a command sequence is complete and the target is ready, WP# can be transitioned.

After WP# is transitioned, the host must wait tWW before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

Ready/Busy#

The ready/busy# (R/B#) signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its die (LUNs) are busy (RDY = 0). A target is ready when all of its die (LUNs) are ready (RDY = 1). Because each die (LUN) contains a status register, it is possible to determine the independent status of each die (LUN) by polling its status register instead of using the R/B# signal (see Status Operations section for details regarding die (LUN) status).

This signal requires a pull-up resistor, R_P, for proper operation. R/B# is HIGH when the target is ready, and transitions LOW when the target is busy. The signal's open-drain driver enables multiple R/B# outputs to be OR-tied. Typically, R/B# is connected to an interrupt pin on the system controller (see READY/BUSY# Open Drain figure below).

It is not permitted to drive or have the NAND R/B# signal HIGH while the NAND V_{CCQ} voltage is below V_{CCQ} Min.

The combination of R_P and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for R_P depends on the system timing requirements. Large values of R_P cause R/B# to be delayed significantly. Between the 10- to 90-percent points on the R/B# waveform, the rise time is approximately two time constants (TC).

$$TC = R \times C$$

Where R = *Rp* (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance. Approximate R_P values using a circuit load of 100pF are provided in Figure 30.

The minimum value for R_P is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CCQ}.

$$Rp = \frac{V_{CCQ}\ (MAX) - V_{OL}\ (MAX)}{IOL + \Sigma il}$$

Where Σil is the sum of the input currents of all devices tied to the R/B# pin.

Figure 29: READY/BUSY# Open Drain

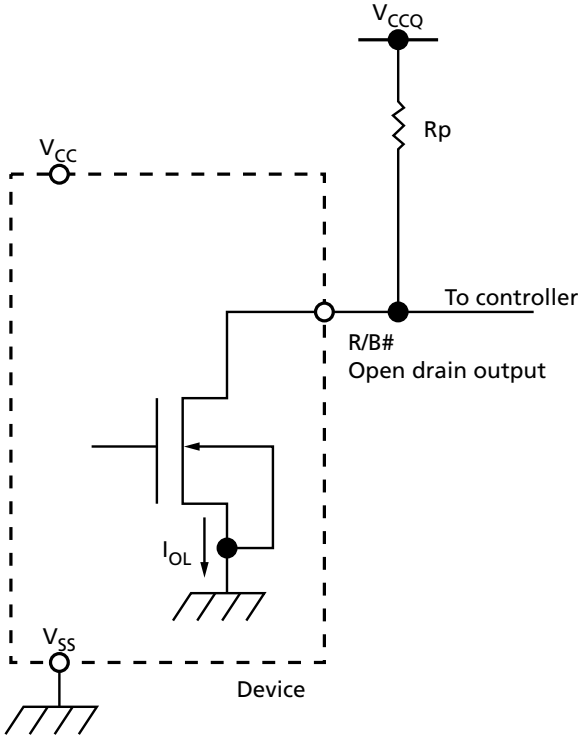
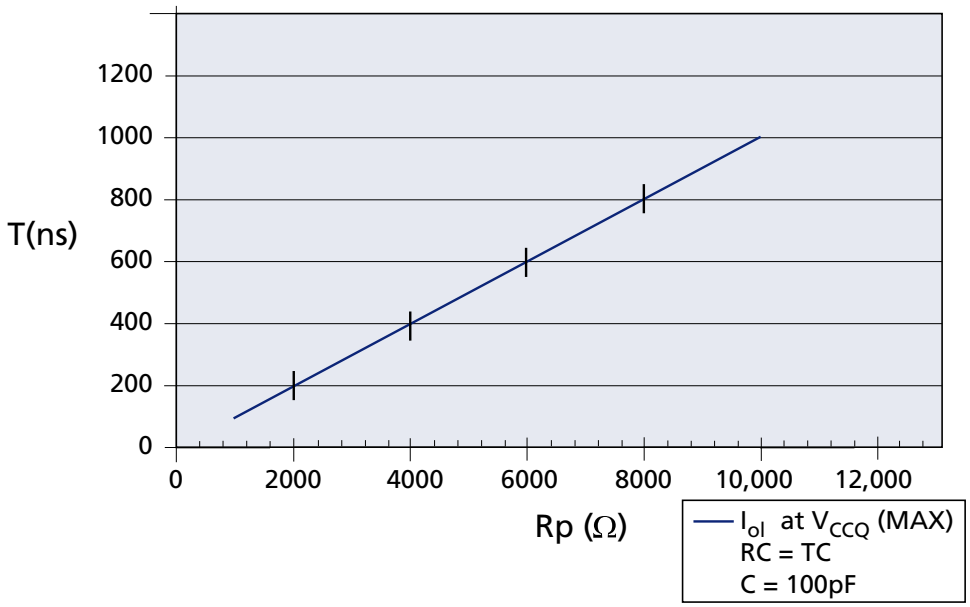


Figure 30: TC vs R_P



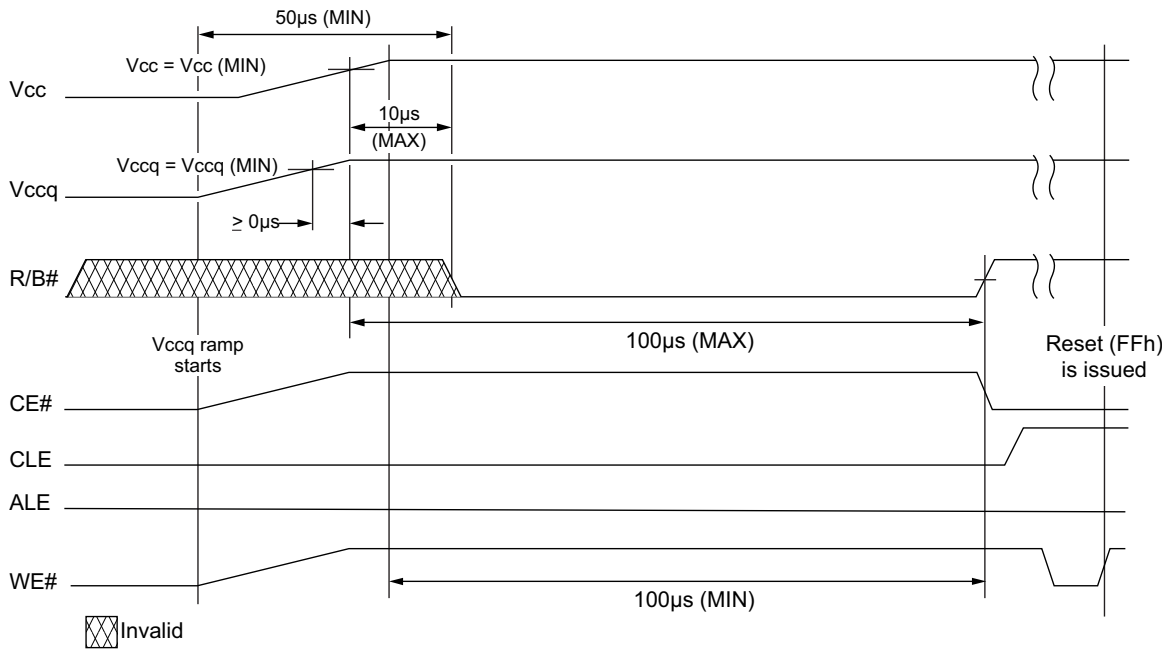
Device Initialization

This section describes the general steps required to power on and initialize the device. This procedure may need to be modified depending on the system configuration. Modifications can be found in the following sections or subsections: Power Cycle and Ramp Requirements, Multi-LUN initialization, V_{PP} initialization, Electronic Mirroring, Activating Interfaces, and Volume Addressing.

When ramping V_{CC} and V_{CCQ}, use the following procedure to initialize the device:

1. Ramp V_{CCQ}.
   - R/B#, RE_t/RE_c, DQ[7:0], and DQS_t/DQS_c signals may be ramped with V_{CCQ} during power-up but not exceed V_{CCQ}
   - CE# and WE# should be ramped with V_{CCQ} during power-up and remain high at least 100µs after both V_{CC} and V_{CCQ} reach a stable voltage
   - ALE and CLE should be low during V_{CCQ} ramp and remain low at least 100µs after both V_{CC} and V_{CCQ} reach a stable voltage
   - When V_{CCQ} = 0V,
     - the host must keep R/B#, RE_t/RE_c, DQS_t/DQS_c signals LOW.
     - the host must keep DQ[7:0] signals LOW or they can be left High-Z.
2. Ramp V_{CC}. V_{CC} may ramp before, simultaneously, or after V_{CCQ}.
3. Wait for R/B# to be valid and HIGH before issuing RESET (FFh) on any target (see Power-On Behavior figure).
   - If monitoring R/B#, the R/B# signal becomes valid when 50µs have elapsed since the beginning the V_{CC} ramp, and 10µs have elapsed since V_{CCQ} reaches V_{CCQ} (MIN) and V_{CC} reaches V_{CC} (MIN). After which the host must wait until R/B# is HIGH.
   - If not monitoring R/B#, the host must wait at least 100µs after V_{CCQ} reaches V_{CCQ} (MIN) and V_{CC} reaches V_{CC} (MIN).
   - The NAND status after the R/B# signal is HIGH after power-on will be F0h (if WP# is HIGH) or 70h (if WP# is LOW) which indicates a first RESET (FFh) command is required to initialize the target. Each LUN draws less than an average of I_{ST} measured over intervals of 1ms until the RESET (FFh) command is issued.
4. Issue a RESET (FFh) command to all targets. Each target will be busy for ^{t}POR. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on.
5. The RESET busy time ^{t}POR can be monitored by polling R/B# or polling the status register of each LUN.
   - Status can be checked using FIXED ADDRESS READ STATUS ENHANCED (71h). Checking status with READ STATUS (70h) or READ STATUS ENHANCED (78h) command is prohibited during ^{t}POR.
   - The host must not issue an additional RESET (FFh) command during ^{t}POR.
6. The host should check initialization result of each LUN after ^{t}POR completes. This can be done with READ STATUS (70h), READ STATUS ENHANCED (78h), or FIXED ADDRESS READ STATUS ENHANCED (71h).
   - If the power-on fails, the status register fail status bit will be updated (SR[0] = 1).
7. The device is now initialized and ready for normal operation. LUN0 of each target is selected by default after power-on.

Figure 31: Power-On Behavior



Note: 1. Disregard V_{CCQ} for devices that use only V_{CC}.

To initialize a discovered target, the following steps shall be taken. The initialization process should be followed for each connected CE# signal, including performing the READ PARAMETER PAGE (ECh) command for each target. Each chip enable corresponds to a unique target with its own independent properties that the host shall observe and subsequently use.

The host should issue the READ PARAMETER PAGE (ECh) command. This command returns information that includes the capabilities, features, and operating parameters of the device. When the information is read from the device, the host shall check the cyclic redundancy code (CRC) to ensure that the data was received correctly prior to taking action on that data.

If the CRC of the first parameter page read is not valid, the host should read redundant parameter page copies. The host can determine whether a redundant parameter page is present or not by checking if the first four bytes contain at least two bytes of the parameter page signature. If the parameter page signature is present, then the host should read the entirety of that redundant parameter page. The host should then check the CRC of that redundant parameter page. If the CRC is correct, the host may take action based on the contents of that redundant parameter page. If the CRC is incorrect, then the host should attempt to read the next redundant parameter page by the same procedure.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. The host may use bit-wise majority or other ECC techniques to recover the contents of the parameter page from the parameter page copies present. When the host determines that a parameter page signature is not present, then all parameter pages have been read.

After successfully retrieving the parameter page, the host has all information necessary to communicate with that target. If the host has not previously mapped defective block information for this target, the host should next map out all defective blocks in the target. The host may then proceed to utilize the target, including erase and program operations.

V_{PP} Initialization

Some NAND Flash devices do not support V_{PP}.

Micron NAND Flash devices support the V_{PP} signal as a way for the host system to enhance NAND array operations by improving power efficiency. When ramping V_{PP}, use the following procedure to initialize the V_{PP} functionality:

1. V_{PP} shall not be ramped HIGH or stay HIGH, above 2V, before V_{CC} (MIN) is reached.
2. V_{PP} must be within its valid voltage range prior to the SET FEATURES (EFh) command to enable the V_{PP} functionality.
3. After V_{PP} is successfully ramped and before V_{PP} functionality can be carried out, the V_{PP} feature must be activated via a SET FEATURES (EFh) command. See the Configurations Operations section for more details.
4. To deactivate V_{PP} functionality without a device power-down, a SET FEATURES (EFh) command must be issued to disable the V_{PP} functionality while V_{PP} is within its valid voltage range.

At power-down, V_{PP} shall ramp LOW, below 2V, before V_{CC} (MIN) is reached.

Volume Addressing

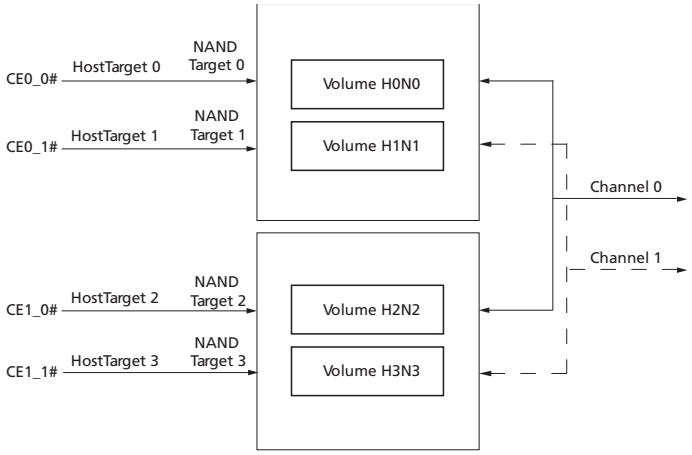
Volume Appointment

If the host desires to have a terminator on a package that does not share a CE# with the selected NAND target, then each package that shares the CE# must have a volume appointed at device initialization using the SET FEATURE (EFh) command using Feature Address 58h: Volume configuration.

Each CE# must have a unique volume address appointed. All LUNs on a CE# must have the same volume address. Once all NAND targets have volume addresses appointed, the appointed volume addresses may be used for termination selection. Volume addressing is not required for operation due to discrete CE# signals; however, the VOLUME SELECT (E1h) command is required for terminator selection when using non-target termination schemes.

During operation, the CE# signal for the selected Volume and for any NAND targets assigned as a terminator for the selected volume need to be brought LOW. When CE# is brought LOW for an unselected volume, all LUNs that are not assigned as terminators for the selected volume are deselected.

Figure 32: Volume Addressing Assignment With Dual Channel Example



Appointing Volume Addresses

To appoint a volume address, the SET FEATURE (EFh) command is issued with a feature address of volume configuration. The volume address is not retained across power cycles; thus, if volume addressing is going to be used it needs to be appointed after each power-on prior to use of the NAND device(s). The volume address is retained when HARD RESET (FDh) command is issued.

Selecting a Volume

After volume addresses have been appointed, every NAND target (and associated LUN) is selected when the associated CE# is pulled LOW. After CE# is held LOW for at least ^{t}CSVOL, the host issues a VOLUME SELECT (E1h) command to indicate the volume (NAND target) that shall execute the next command issued.

Multiple Volume Operation Restrictions

Volumes are independent entities. A multiple volume operation is when two or more Volumes are simultaneously processing commands. Before issuing a command to an unselected volume, CE# shall be pulled HIGH for a minimum of ^{t}CEH, and the VOLUME SELECT (E1h) command shall then be issued to select the volume to issue a command to next. While commands (including multi-LUN oper-

ations) are being performed on the selected volume, a VOLUME SELECT (E1h) command is not required.

Issuing the same command to multiple volumes at the same time is not supported.

For a LUN level command (for example, READ, PROGRAM), the host may select a different volume during a data input or data output operation and then resume the data transfer operation at a later time for a LUN level command, however, when interrupting data input operations with a VOLUME SELECT (E1h) command, the host is required to issue an 11h command prior to the issuance of the VOLUME SELECT (E1h) command. When re-selecting a Volume and associated LUN to complete the data input or data output operation, the following actions are required:

- Data input: The host shall wait ^{t}CCS and then issue a CHANGE ROW ADDRESS (85h) command prior to resuming data input.
- Data output: The host shall issue a CHANGE READ COLUMN ENHANCED (06h-E0h) or RANDOM DATA OUT (00h-05h-E0h) command prior to resuming data output.

For a target level command (GET FEATURES (EEh), SET FEATURES (EFh)), the host shall complete all data input or data output operations associated with that command prior to selecting a new volume.

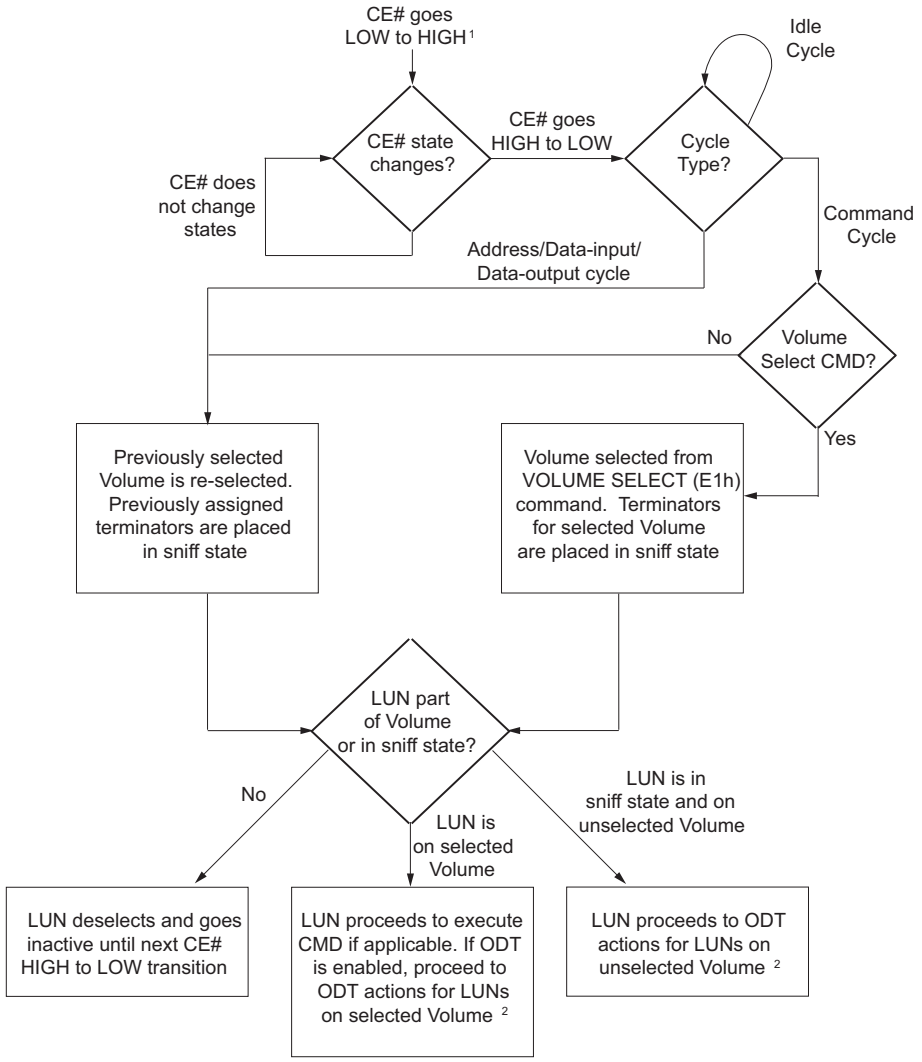
A VOLUME SELECT (E1h) command shall not be issued during the following atomic portions of the COPYBACK, READ, PROGRAM, and ERASE operations:

- READ operations:
  - IWL READ (00h-20h)
  - READ PAGE (00h-30h)
  - COPYBACK READ (00h-35h)
  - READ PAGE MULTI-PLANE (00h-32h)
  - READ PAGE CACHE RANDOM (00h-31h)
- PROGRAM operations, note: The host may interrupt a program data input burst sequence, select another volume and resume the data input burst at a later time, however an 11h command needs to be issued prior to the VOLUME SELECT (E1h) command that selects the other volume. To resume the interrupted program data input sequence, a VOLUME SELECT (E1h) command needs to be given to select the volume where the program data input sequence was interrupted, the host shall then wait ^{t}CCS before issuing a CHANGE ROW ADDRESS (85h) command to resume the data input sequence:
  - PROGRAM PAGE (80h-10h)
  - PROGRAM PAGE MULTI-PLANE (80h-11h)
  - PROGRAM PAGE CACHE (80h-15h)
  - COPYBACK PROGRAM (85h-10h)
  - COPYBACK PROGRAM MULTI-PLANE (85h-11h)
- ERASE operations:
  - ERASE BLOCK (60h-D0h)
  - ERASE BLOCK MULTI-PLANE (60h-D1h or 60h-60h-D0h)

Volume Reversion

When using volume addressing, the LUNs shall support Volume reversion. Specifically, if CE# is transitioned from HIGH to LOW and a Volume Select is not the first command, then the LUN shall revert to the previously Selected, Sniff, and Deselected states based on the last specified volume address. If on-die termination is enabled there are additional actions described within On Die Termination (ODT) section.

Figure 33: Volume Reversion Behavioral Flow



Notes: 1. This state is entered asynchronously when CE# transitions from LOW to HIGH.
2. ODT actions for LUNs on a selected Volume are specified in Bus Operation NV-DDR3 Interface, Matrix Termination section. ODT actions for LUNs on an unselected Volume are specified in Bus Operation NV-DDR3 Interface, Matrix Termination section.

Data Training

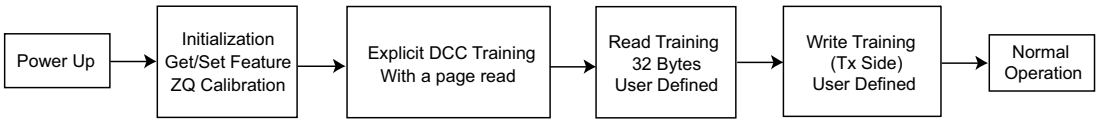
For NAND device interface speeds higher than 800 MT/s, data training is required to assure interoperability. The data training features includes duty cycle correction (DCC), read training (controller based), and write training transceiver (Tx) side. Data training is supported by NAND devices operating over 800 MT/s in heavily loaded systems.

It is highly recommended that users follow the training sequences defined in the data sheet. It is prohibited to insert any other command or operation in the middle of a training sequence. Adding other commands or operations in the middle of a training sequence may cause training failures. Users may do training during normal operations except when the part is in Program Suspend (84h) or Erase Suspend (61h) state, but should still follow the procedures defined for each data training feature.

DCC training is a feature for the NAND to compensate the duty cycle mismatch of RE_t/RE_c signals. Read/write DQ training is a feature for the host to align DQS and DQ signals caused by unmatched DQS path.

The following diagram shows each training sequence after power-on. Initialization shall be done before training at slower interface speeds such as high-speed Interface setting, driver strength setting and ZQ calibration. The host shall operate DCC training before read/write DQ training.

Figure 34: Data Training Sequence Diagram



DCC Training

Explicit DCC training shall be performed after ZQ calibration is completed. Explicit DCC training shall be supported by NAND devices operating over 800 MT/s. Explicit DCC training can be enabled via feature address 20h: DCC training and write DQ training (Tx side). Depending on the ODT Self-Termination usage on the CE#, Explicit DCC Training may be done one LUN at a time (Single LUN DCC Training) or in parallel (Parallel DCC Training).

Single LUN DCC Training

When the signal integrity requirements of a CE# requires that ODT Self-Termination is enabled (via FA 02h P1[7:4]) on the LUNs of the CE#, the system is constrained to perform Single LUN DCC Training for that CE#. With Single LUN DCC Training, the LUNs on the CE# are trained one at a time till all the LUNs of the CE# have been trained.

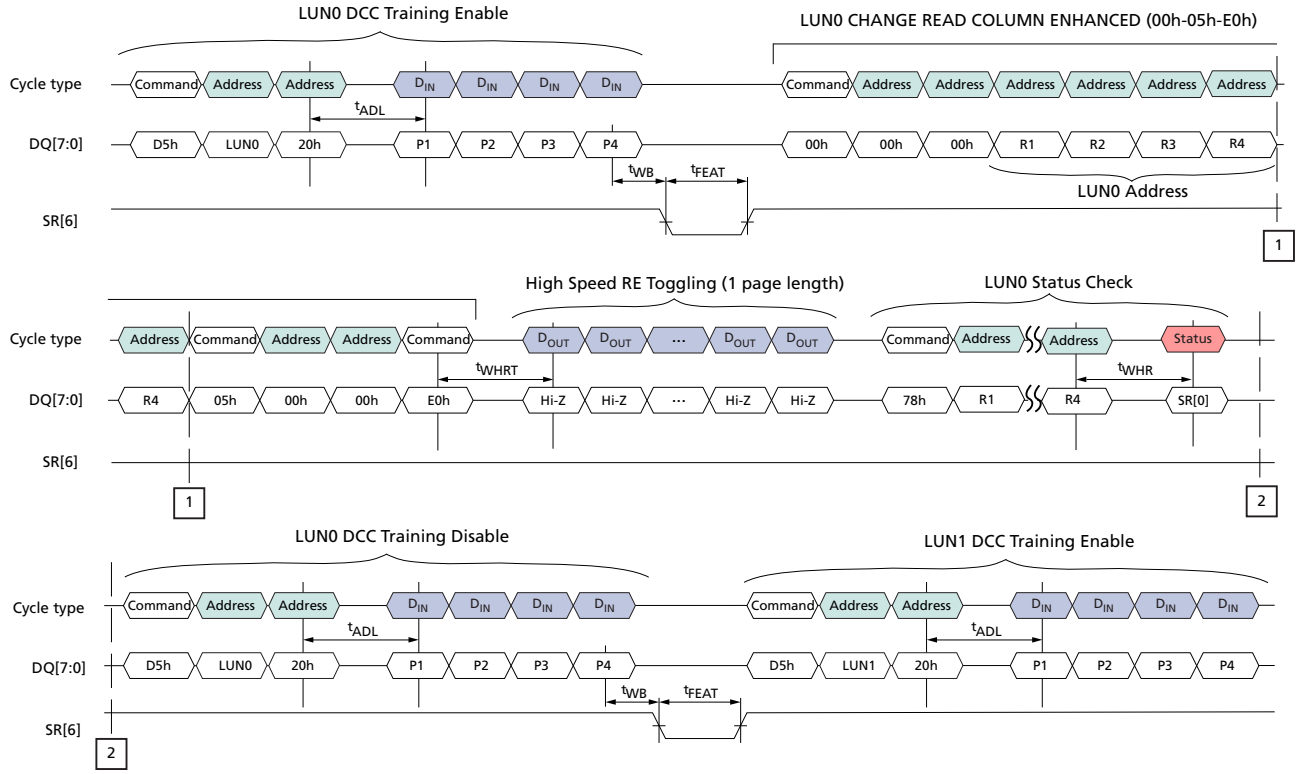
To perform Single LUN DCC Training, the host shall issue the SET FEATURE by LUN (D5h) command with the address of the LUN, setting FA 20h P1[0]= 1. After ^{t}FEAT, the host shall issue the CHANGE READ COLUMN ENHANCED (00h-05h-E0h) command with the address of the LUN that is being trained in the address field of the command. Note that CHANGE READ COLUMN ENHANCED (06h-E0h) is not supported during DCC Training. The host shall then toggle data output cycles from the device (that is, toggle RE_t/RE_c) for a page size length. During the time that RE_t/RE_c are toggled by the host for a page size length, the LUN's DQ and DQS pins will be in the High-Z state, the data from the LUN will be invalid and shall be ignored by the host.

After sending RE_t/ RE_c for a page size length, Status Check shall then be performed to confirm whether DCC Training passed or failed via SR[0] for that LUN. If the status is a fail, the host may adjust any of its settings and issue the CHANGE READ COLUMN ENHANCED (00h-05h-E0h) command and resend RE_t/RE_c signals to calibrate the LUN again. If no passing DCC training solution is found for

the LUN, the host may decide to continue running the failing LUN through the rest of the training flow or through normal operations, but retire it if no reliable read solution was found during read training or the read error threshold from the LUN during normal operations is too high.

To end DCC Training for the LUN, the host shall issue the SET FEATURE by LUN (D5h) command to clear FA 20h P1[0] to 0. After ^{t}FEAT, DCC training for the LUN is complete and the host then proceeds to the DCC training of the next untrained LUN on the CE# till all the LUNs on the CE# have been trained.

Figure 35: Single LUN DCC Training Using SET FEATURE by LUN (D5h)



Notes: 1. During the data output cycles after the E0h command, the device DQ and DQS pins for the LUN under training will be in the High-Z state. Thus, the data for those data output cycles will be invalid and shall be ignored by the host.
2. Refer to the Device and Array Organization section for more details on R1, R2, R3, and R4. For Single LUN DCC Training the R1, R2, R3, and R4 address fields during the CHANGE READ COLUMN ENHANCED (00h-05h-E0h) command sequence shall contain the address of the LUN that is being trained.

Parallel DCC Training

Parallel DCC Training is only allowed when the signal integrity requirements of a CE# does not require ODT Self-Termination to be used and the ODT Self-Termination settings for all the LUNs on the CE# are disabled (ie. FA02h P1[7:4] = 0h). With Parallel DCC Training, all the LUNs on the CE# are trained together, allowing a reduction in DCC training time.

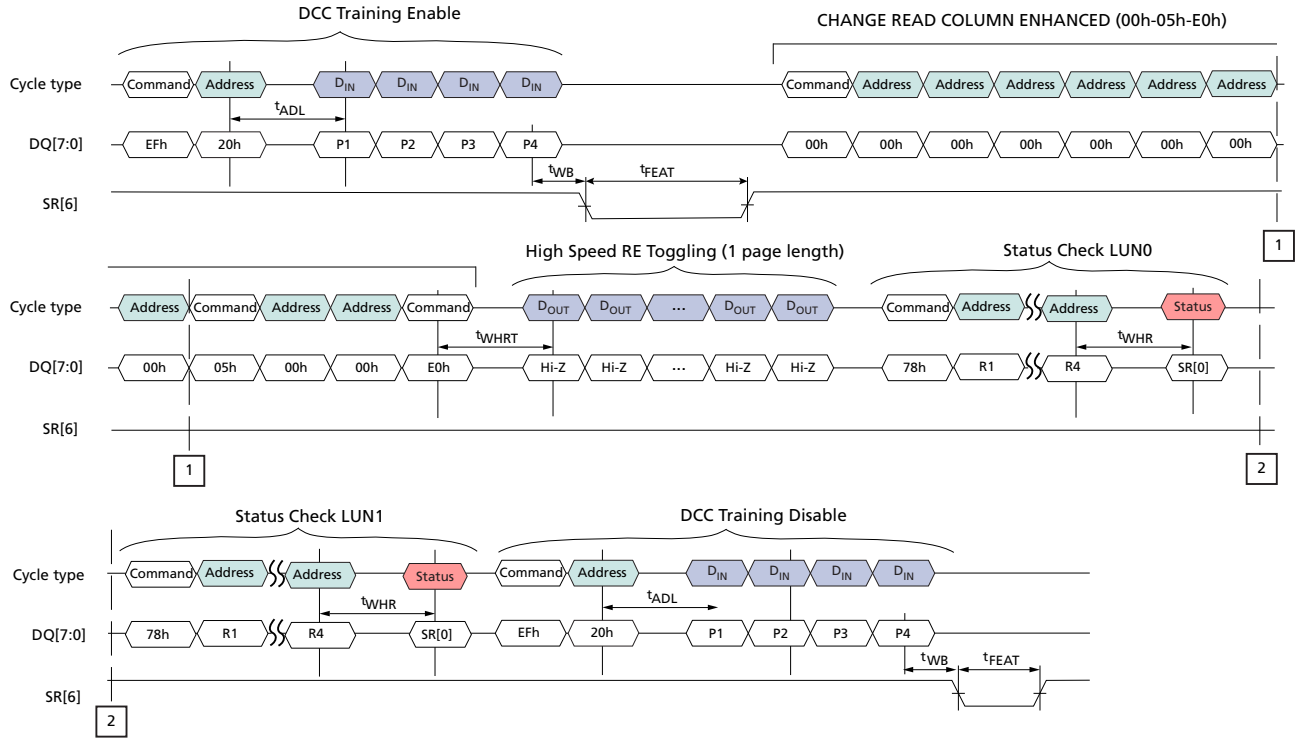
To perform Parallel DCC Training, the host shall issue a SET FEATURE (EFh) command to the CE#, setting FA 20h P1[0] = 1. After ^{t}FEAT, the host shall issue a CHANGE READ COLUMN ENHANCED (00h-05h-E0h) command with the addresses filled with 00h. Note that CHANGE READ COLUMN ENHANCED (06h-E0h) is not supported. The host shall then toggle data output cycles from the device (that is, toggle RE_t/RE_c) for a page size length. During the time that RE_t/RE_c are toggled by the

host for a page size length, the DQ and DQS pins of all LUNs on the CE# will be in the High-Z state, the data will be invalid and shall be ignored by the host.

After sending RE_t/ RE_c for a page size length, Status Check shall then be performed on each LUN to confirm whether DCC Training passed or failed via SR[0]. If the status on a LUN is a fail, the host must first end Parallel DCC training by issuing a SET FEATURE (EFh) command to the CE#, clearing FA 20h P1[0] = 0 and waiting ^{t}FEAT.

After exiting Parallel DCC Training, the host may proceed to perform Single LUN DCC training on the failing LUN. If no passing Single LUN DCC training solution is found, the host may decide to continue running the failing LUN through the rest of the training flow or through normal operations, but retire it if no reliable read solution was found during read training or the read error threshold from the LUN during normal operations is too high.

Figure 36: Parallel DCC Training Using SET FEATURE (EFh)



Notes: 1. During the data output cycles after the E0h command, the device DQ and DQS pins will be in the High-Z state. Thus, the data for those data output cycles will be invalid and shall be ignored by the host.
2. For Parallel DCC Training, the host shall fill all address fields for the CHANGE READ COLUMN ENHANCED (00h-05h-E0h) command sequence with 00h.

Table 14: Feature Address 20h: DCC Training and Write DQ Training (Tx Side)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Explicit DCC Training	Disabled (default)								0	0b	1, 2
	Enable								1	1b	

Table 14: Feature Address 20h: DCC Training and Write DQ Training (Tx Side) (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Factory Setting	Disable (default)						0			0b	5
	Enable						1			1b	
Reserved		0	0	0	0	0		0		00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Write Training Tx Data Pattern Size	See note					0	0	0	1	0001b	3
Read Training Data Pattern Length	See note (32 bytes only)				1					1b	4
Reserved		0	0	0						000b	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. Explicit DCC training shall be disabled (feature address = 20h P1[0] = 0) during power-up.
2. Host can set DCC training enable/disable to disable if host does not need DCC for low frequency operations.
3. P3[3:0] for Write Training TX data size. Bit values are fixed and cannot be altered. However, Micron parts are not sensitive to this field, and can support any Write Training Tx data size that is a multiple of 16 bytes and less than one page in length.
4. P3[4] for Data Pattern Length for Read Training [1: 32 Bytes only]. Bit value is fixed and cannot be altered. Micron parts only support a Read Training Data Pattern Length of 32 bytes.
5. If Factory Setting is set to 1 (feature address = 20h P1[2] = 1) after DCC completion, then the default settings for output would be reset to the factory settings.

DCC Training Reset Behavior

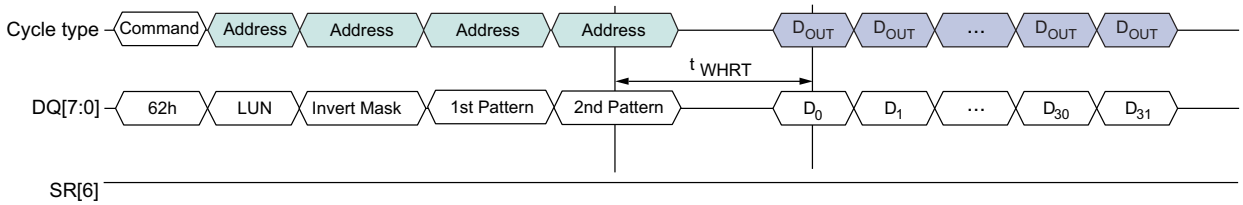
- RESET (FFh/FAh) will reset FA 20h but will not reset the internal DCC settings from the last DCC training. After RESET (FFh/FAh), the device will continue to use the DCC settings from the last DCC training sequence. A HARD RESET (FDh) command will reset both FA 20h and the internal DCC settings back to power-on default values.
- If host interrupts the DCC training of a LUN with a RESET (FFh/FAh), then results are not guaranteed and DCC training must be repeated for that LUN.

Read DQ Training

Read DQ training is a function that outputs a 32 bit user defined pattern on each of the DQ pins. It means a total of 32 bytes is output by the NAND device.

Read DQ training can be enabled by issuing the READ DQ TRAINING (62h) command followed by LUN address, and then three address cycles. Three address cycles are the first address (8-bit invert mask), second address (the first 8-bit pattern) and the third address (the second 8-bit pattern).

Figure 37: Read DQ Training



The Read Training User Defined Pattern Example Table below provides a detailed data pattern example (for example, the first address = 35h, second address = 5Ah, and the third address = 82h). For the first address (8-bit invert mask), DQ0–7 represent the 8-bit invert mask, where 1 indicates "Inverse" for the setting. The second address (the first 8-bit pattern) is represented by bytes 0–7, and the third address (the second 8-bit pattern) is represented by bytes 8–15 respectively. If 1 is indicated by a bit in the first address, the DQx corresponding to that bit shall be inverted and the NAND device outputs data pattern designated by the second and the third addresses masked I/O. Note for the second address (the first 8-bit pattern), byte 0 starts with the least significant bit (LSB) of the input address, and byte 7 ends with the most significant bit (MSB) of the input address. Similarly, for the third address (the second 8-bit pattern), byte 8 starts with the LSB of the input address, and byte 15 ends with the MSB of the input address. Since a 32 byte pattern is required, DQ0–DQ3 data from byte 0–15 will swap with DQ4–DQ7 data from byte 0–15 for byte 16–31 data input. That is DQ0–DQ3 from byte 0–15 is the DQ4–DQ7 data input for byte 16–31, and DQ4–DQ7 from byte 0–15 is the DQ0–DQ3 data input for byte 16–31.

Table 15: Read Training User Defined Pattern Example Table (Inverse Setting and Bytes 0–15)

Pin	Inverse Setting	Bytes 0–7								Bytes 8–15							
	1st Address: 8-Bit Invert Mask	2nd Address: 1st 8-Bit Pattern								3rd Address: 2nd 8-Bit Pattern							
	For Example: 35h	For Example: 5Ah								For Example: 82h							
DQ0	1 (Inverse)	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ1	0	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ2	1 (Inverse)	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ3	0	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ4	1 (Inverse)	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ5	1 (Inverse)	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ6	0	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ7	0	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1

Table 16: Read Training User Defined Pattern Example Table (Bytes 16–31)

Pin	Bytes 16–31															
	Swap DQ0–DQ3 With DQ4–DQ7 from 0–15 Bytes															
DQ0	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ2	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ3	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1

Table 16: Read Training User Defined Pattern Example Table (Bytes 16–31)

Pin	Bytes 16–31															
	Swap DQ0–DQ3 With DQ4–DQ7 from 0–15 Bytes															
DQ4	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ5	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ6	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ7	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1

Write DQ Training (Tx Side)

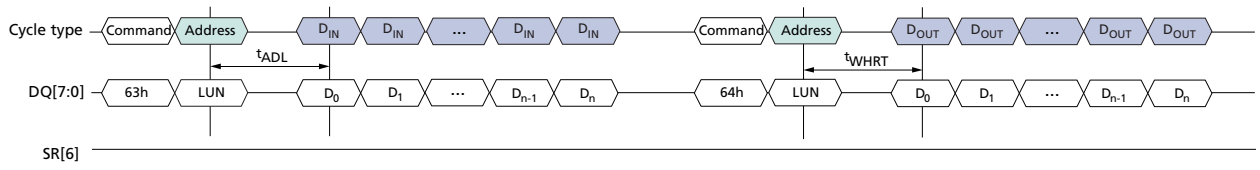
To perform write training at Tx side, the controller shall issue WRITE DQ TRAINING - Tx Side (63h) command followed by LUN address. After issuing LUN address, the host shall input data pattern and confirm whether the input is successfully done by checking the output by NAND in following sequence.

Data sizes for write DQ is predefined by NAND. The host shall recognize the data sizes by issuing GET FEATURE by LUN (D4h) command with feature address = 20h. The write training data size is given in the feature address 20h: DCC training and write training (Tx Side) table. The host shall input and output the data based on the write training data size.

After issuing the 63h command followed by LUN address to write the data, the data can be read back with WRITE DQ TRAINING - Tx Read Back (64h) command followed by the same LUN address and the results shall be compared with "expected" data to see if further training (DQ delay) is needed.

If fewer data than predefined data bytes are written, then unwritten registers will have undefined data when read back. If over predefined data bytes read were executed, the data are also undefined and invalid.

Figure 38: Write DQ Training (Tx Side)



Electronic Mirroring

Electronically mirrored DQ[7:0] pinout is available in order to assist in optimizing printed circuit board (PCB) layout by assisting two-sided (clamshell) designs in reducing the complexity and the number of signal routing layers between the top and bottom side of the PCB. This ability for electronic mirrored DQ[7:0] pinout also assists in reducing the vertical profile of a two-sided system. Only the DQ[7:0] signals have the ability to be changed by electronic mirrored functionality, all other NAND signals remain static.

See Example PCB Layout of a Two-Sided System without Electronic Mirroring of DQ[7:0] and Example PCB Layout of a Two-Sided System with Electronic Mirroring of DQ[7:0] as examples of how packages in the default non-mirrored DQ[7:0] pinout and the mirrored DQ[7:0] pinout could be used in a two-sided PCB system.

Figure 39: Example PCB Layout of a Two-Sided System without Electronic Mirroring of DQ[7:0]

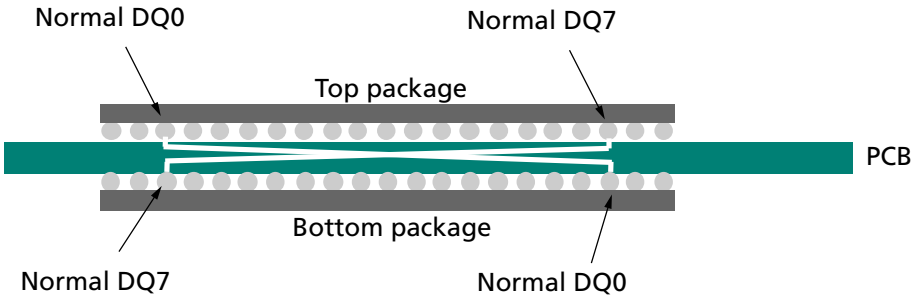
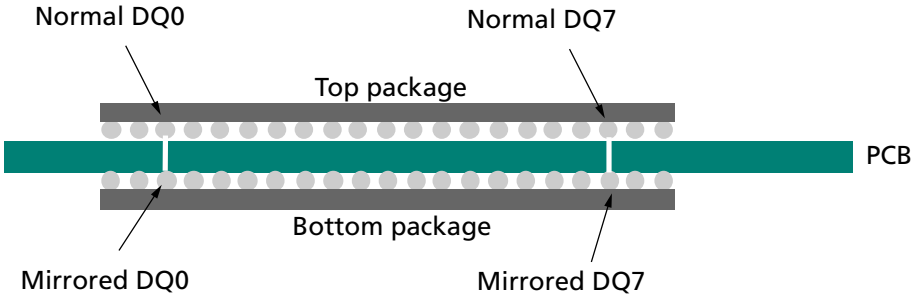


Figure 40: Example PCB Layout of a Two-Sided System with Electronic Mirroring of DQ[7:0]



The mirror and non-mirrored packages are physically the same with same internal bond connections. Based on how the first READ STATUS (70h) command is decoded, the LUNs internally are electrically configured to be mirrored or non-mirrored.

The READ STATUS (70h) command is used to set devices into the mirrored DQ[7:0] pinout configuration. The command can be issued before or after the RESET (FFh) command, but if after, the host must wait for ^{t}POR. The NAND bus of the mirrored DQ[7:0] pin configuration die will see the 70h command as “0Eh”. That NAND device will decode the “0Eh” as the indication to configure itself into the mirrored mode. Setting die into the mirrored configuration is done only once per target (CE#) or volume such that once issued and interpreted as “E0h”, the device will remain in the mirrored DQ[7:0] mode until device power-down.

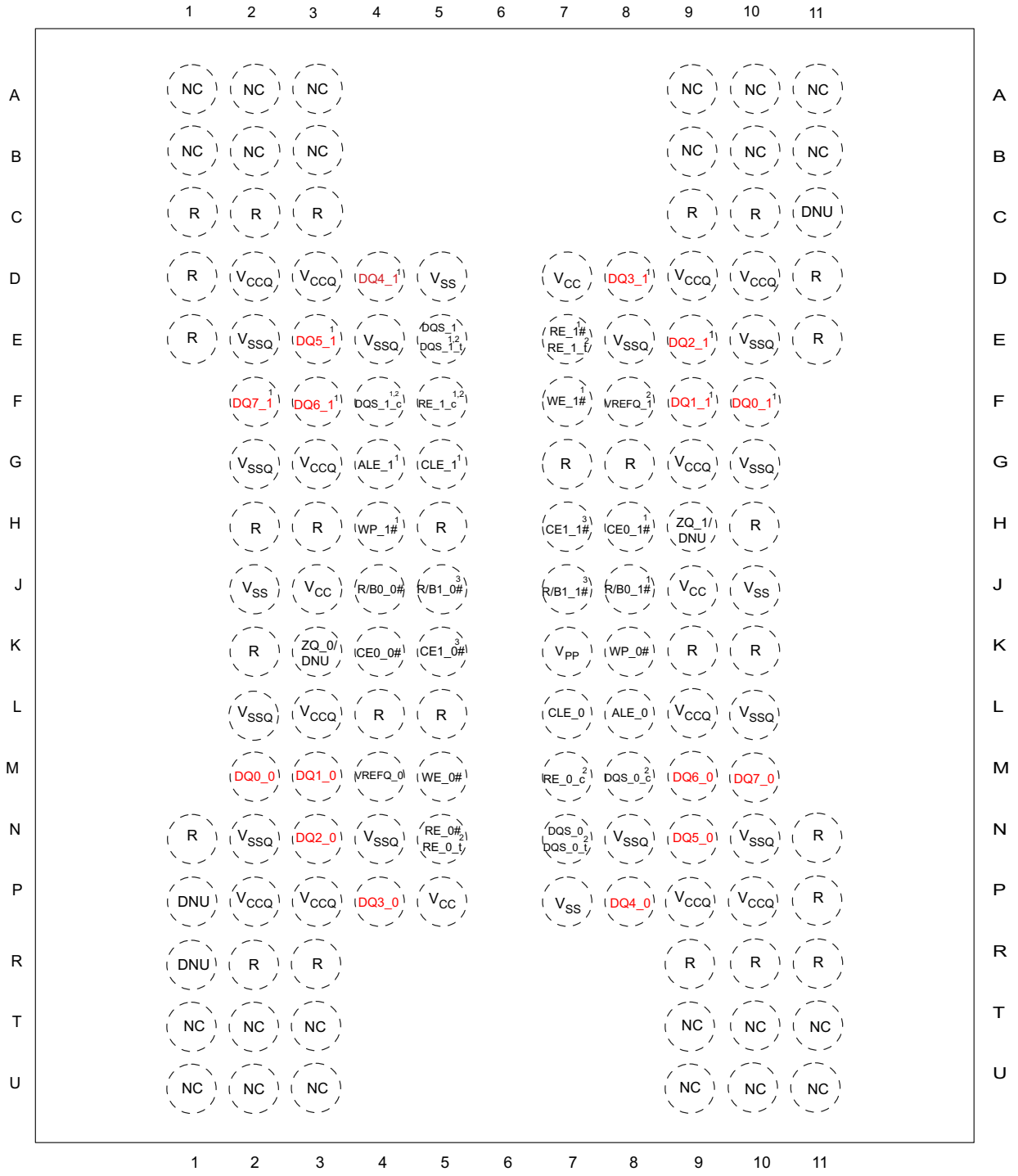
Only the 132-ball, 152-ball BGA, and 154-ball BGA packages offer electronic mirroring operations. The 272-ball and 252-ball BGA package will not support electronic mirroring due to the limitation of DQ[7:0] signal assignment ordering.

See the figure below as an example of how a package in the mirrored DQ[7:0] pinout changes signal assignments for the DQ[7:0] signals.

A HARD RESET (FDh) command will not change a device from the mirrored pinout configuration to the non-mirrored pinout configuration.

The ODT CONFIGURE (E2h) command requires special handling for LUNs operating in mirrored DQ[7:0] mode. Refer to the ODT CONFIGURE (E2h) section.

Figure 41: Example of 132-Ball BGA Package in Mirrored DQ[7:0] Pinout



Note: 1. Note the DQ[7:0] signals highlighted in red for the mirrored pinout configuration in comparison to the default non-mirrored pinout configuration. See the Signal Assignments section for the default non-mirrored pinout configuration for this package.

Activating Interfaces

After performing the steps under Device Initialization, the NV-DDR3 interface is active for all targets on the device. No SET FEATURES (EFh) command is required to activate the NV-DDR3 interface after device initialization process is complete. Any SET FEATURE (EFh) command to feature address 01h to the data interface bits when in the NV-DDR3 interface will not cause the NAND device to exit the NV-DDR3 interface.

It is recommended that settings for the NV-DDR3 interface be configured. Specifically:

- As the NAND device powers-on directly into the NV-DDR3 interface, it is recommended that the host operate in a slower NV-DDR3 timing mode (such as timing mode 2) after power-on to configure the NAND device properly for system signal integrity purposes before transitioning to faster NV-DDR3 timing modes.
- If matrix on-die termination (ODT) is used, the appropriate ODT CONFIGURE (E2h) commands should be issued.

Command Definitions

Commands other than those defined in the Command Set table are illegal and shall not be issued to the NAND.

Table 17: Command Set

Command	Command Cycle #1	Number of Valid Address Cycles #1	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles #2	Command Cycle #3	Valid While Selected LUN is Busy[2]	Valid While Other LUNs are Busy[3]	Notes
Reset Operations									
RESET	FFh	0	–	–	–	–	Yes	Yes	1
HARD RESET	FDh	0	–	–	–	–		Yes	1
RESET LUN	FAh	4	–	–	–	–	Yes	Yes	1
Identification Operations									
READ ID	90h	1	–	–	–	–			1, 4
READ PARAMETER PAGE	ECh	1	–	–	–	–			1
READ UNIQUE ID	EDh	1	–	–	–	–			1
Configuration Operations									
SLC MODE LUN ENABLE	3Bh	0	–	–	–	–		Yes	1
VOLUME SELECT	E1h	1	–	–	–	–			1
ODT CONFIGURE	E2h	2	4	–	–	–			1
GET FEATURES	EEh	1	–	–	–	–			1, 4
SET FEATURES	EFh	1	4	–	–	–			1, 5
GET FEATURES by LUN	D4h	2	–	–	–	–		Yes	1, 4
SET FEATURES by LUN	D5h	2	4	–	–	–		Yes	1, 5
ZQ CALIBRATION LONG	F9h	1	–	–	–	–		Yes	1
ZQ CALIBRATION SHORT	D9h	1	–	–	–	–		Yes	1
Status Operations									
READ STATUS	70h	0	–	–	–	–	Yes		1

Table 17: Command Set (Continued)

Command	Command Cycle #1	Number of Valid Address Cycles #1	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles #2	Command Cycle #3	Valid While Selected LUN is Busy[2]	Valid While Other LUNs are Busy[3]	Notes
FIXED ADDRESS READ STATUS ENHANCED	71h	1	–	–	–	–	Yes	Yes	1
READ STATUS ENHANCED	78h	4	–	–	–	–	Yes	Yes	1
EXTENDED STATUS REGISTER READ	79h	4	–	–	–	–	Yes	Yes	1
Column Address Operations									
CHANGE READ COLUMN	05h	2	–	E0h	–	–		Yes	1, 10
CHANGE READ COLUMN ENHANCED (ONFI)	06h	6	–	E0h	–	–		Yes	1, 10
CHANGE READ COLUMN ENHANCED (JEDEC)	00h	6	–	05h	2	E0h		Yes	1, 10
CHANGE WRITE COLUMN	85h	2	Optional	–	–	–		Yes	1
CHANGE ROW ADDRESS	85h	6	Optional	11h (Optional)	–	–		Yes	1, 6, 10
Read Operations									
READ MODE	00h	0	–	–	–	–		Yes	1
READ PAGE	00h	6	–	30h	–	–		Yes	1, 7, 10
IWL READ	00h	6	–	20h	–	–		Yes	1, 10
READ PAGE MULTI-PLANE	00h	6	–	32h	–	–		Yes	1, 10
READ PAGE CACHE SEQUENTIAL	31h	0	–	–	–	–		Yes	1, 8

Table 17: Command Set (Continued)

Command	Command Cycle #1	Number of Valid Address Cycles #1	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles #2	Command Cycle #3	Valid While Selected LUN is Busy[2]	Valid While Other LUNs are Busy[3]	Notes
READ PAGE CACHE RANDOM	00h	6	–	31h	–	–		Yes	1, 7, 8, 10
READ PAGE CACHE LAST	3Fh	0	–	–	–	–		Yes	1, 8
READ OFFSET PREFIX	2Eh	3	–	–	–	–		Yes	1
SINGLE BIT SOFT BIT READ PAGE	00h	6	–	34h	–	–		Yes	1, 10
Program Operations									
PROGRAM PAGE	80h	6	Yes	10h	–	–		Yes	1, 10
PROGRAM PAGE MULTI-PLANE	80h	6	Yes	11h	–	–		Yes	1, 10
PROGRAM PAGE CACHE	80h	6	Yes	15h	–	–		Yes	1, 9, 10
PROGRAM SUSPEND	84h	6	–	–	–	–	Yes	Yes	1
PROGRAM RESUME	13h	6	–	–	–	–		Yes	1
Erase Operations									
ERASE BLOCK	60h	4	–	D0h	–	–		Yes	1, 10
ERASE BLOCK MULTI-PLANE (ONFI)	60h	4	–	D1h	–	–		Yes	1, 10
ERASE BLOCK MULTI-PLANE (JEDEC)	60h	4	–	60h	4	D0h		Yes	1, 10
ERASE SUSPEND	61h	4	–	–	–	–	Yes	Yes	1
ERASE RESUME	D2h	–	–	–	–	–		Yes	1
Copyback Operations									
COPYBACK READ	00h	6	–	35h	–	–		Yes	1, 7, 10
COPYBACK PROGRAM	85h	6	Optional	10h	–	–		Yes	1, 10

Table 17: Command Set (Continued)

Command	Command Cycle #1	Number of Valid Address Cycles #1	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles #2	Command Cycle #3	Valid While Selected LUN is Busy[2]	Valid While Other LUNs are Busy[3]	Notes
COPYBACK PROGRAM MULTI-PLANE	85h	6	Optional	11h	–	–		Yes	1, 10
Data Training Operations									
READ DQ TRAINING	62h	4	Yes	–	–	–			1
WRITE DQ TRAINING (Tx)	63h	1	Yes	64h	1	–			1, 10

Notes: 1. Commands other than those defined in the Command Set table are illegal and shall not be issue to the NAND.
2. Busy means RDY = 0.
3. These commands can be used for interleaved die (multi-LUN) operations.
4. The READ ID (90h), GET FEATURES (EEh), and GET FEATURES by LUN (D4h) commands output identical data on rising and falling DQS edges.
5. The SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands requires data transition prior to the rising edge of DQS, with identical data for the rising and falling edges.
6. Command cycle #2 of 11h is conditional. See CHANGE ROW ADDRESS (85h) for more details.
7. This command can be preceded by READ PAGE MULTI-PLANE (00h-32h) command to accommodate a maximum simultaneous multi-plane array operation.
8. Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE-series command; otherwise, it is prohibited.
9. Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise, it is prohibited.
10. For command sets which include two command cycles where a confirm command is required (that is, 00h-30h, 80h-10h, and so forth), no other command is allowed between setup and confirm commands except the following:
    - RESET (FFh, FAh, FDh) commands
    - 85h can be issued between 80h/85h and 10h/15h commands

Table 18: Read Assist Features

Command / Feature Name	Description
Read Offset Prefix	2Eh command
Address Cycle Read Retry	7th address cycle
Auto Read Calibration (ARC), ARC persistence	Feature Address 96h
Single Bit Soft Bit Read (SBSBR)	00h-34h

Reset Operations

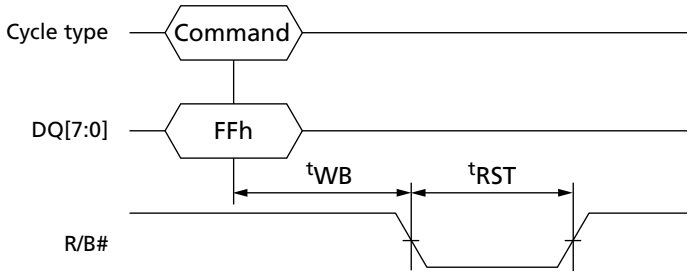
RESET (FFh)

The RESET (FFh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all die (LUNs), even when they are busy.

When FFh is written to the command register, the target goes busy for ^{t}RST. During ^{t}RST, the selected target (CE#) discontinues all array operations on all die (LUNs). All pending single- and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more die (LUNs), the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are valid.

RESET (FFh) must be issued as the first command to each target following power-up (see Device Initialization). Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET. To determine when each LUN on the target is ready, use FIXED ADDRESS READ STATUS ENHANCED (71h).

Figure 42: RESET (FFh) Operation



RESET LUN (FAh)

The RESET LUN (FAh) command is used to put a particular LUN on a target into a known condition and to abort command sequences in progress. This command is accepted by only the LUN addressed by the RESET LUN (FAh) command, even when that LUN is busy.

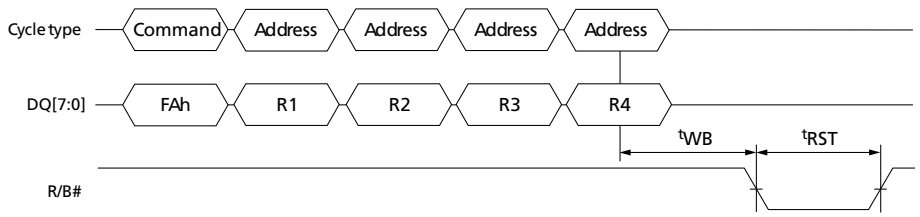
When FAh is written to the command register, the addressed LUN goes busy for ^{t}RST. During ^{t}RST, the selected LUN discontinues all array operations. All pending single- and multi-plane operations are canceled. If this command is issued while a PROGRAM or ERASE operation is occurring on the addressed LUN, the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are valid.

During or after ^{t}RST, the host can poll each LUN's status register.

The RESET LUN (FAh) command is prohibited when in the OTP mode of operation.

The RESET LUN (FAh) command can only be issued to a target (CE#) after the RESET (FFh) command has been issued as the first command to a target following power-up.

Figure 43: RESET LUN (FAh) Operation



HARD RESET (FDh)

The HARD RESET (FDh) command is used to put a particular die (LUN) on a target into a known condition similar to that of a power-on initialized state. The HARD RESET (FDh) command is accepted by only the LUN previously selected by a READ STATUS ENHANCED (78h) command. The host is required to issue a READ STATUS ENHANCED (78h) command prior to issuing the HARD RESET (FDh) command, there should be no other NAND commands after the READ STATUS ENHANCED (78h) command and before the HARD RESET (FDh) command issued by the host. The HARD RESET (FDh) command is only permitted to be issued when the selected LUN is not in a busy state (RDY = 1, ARDY = 1).

HARD RESET (FDh) performs a initialization to the die (LUN) similar to the initialization performed during the first RESET (FFh) command at device power-on. All target LUN parameters and configurations shall be initialized to default values. The target LUN is chosen by the host issuing a READ STATUS ENHANCED (78h) command prior to issuing the HARD RESET (FDh) command. The HARD RESET (FDh) operation is completed within ^{t}POR. After ^{t}POR, the data register and cache register contents of the previously selected LUN that carried out the HARD RESET (FDh) operation are invalid.

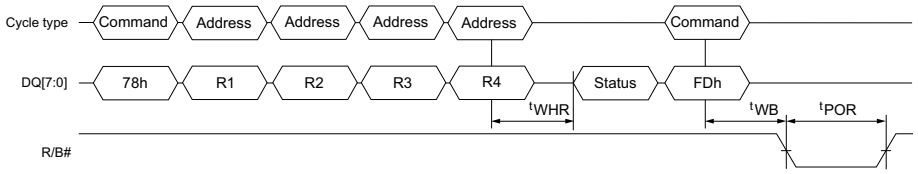
In shared CE# configuration, only the selected LUN shall perform the HARD RESET (FDh) command. The host is required to issue the READ STATUS ENHANCED (78h) command prior to issuing the HARD RESET (FDh) command to select LUN to perform the HARD RESET (FDh) operation.

During or after ^{t}POR, the host can poll each LUN's status register. A status command is only valid 5µs after HARD RESET (FDh) is issued, incorrect status may result if status command is issued within 5µs of HARD RESET (FDh) command. The only status command supported during the HARD RESET (FDh) ^{t}POR time for all LUNs on a target (CE#) is the FIXED ADDRESS READ STATUS (71h) command.

The HARD RESET (FDh) command is prohibited when in the OTP mode of operation.

The HARD RESET (FDh) command can only be issued to a target (CE#) after the RESET (FFh) command has been issued as the first command to a target following power-up. A HARD RESET (FDh) command will not change a device from the mirrored pinout configuration to the non-mirrored pinout configuration. A HARD RESET (FDh) command will change all feature addresses back to their default values for the target LUN with the exception of previously assigned Volume configuration (Feature Address 58h).

Figure 44: HARD RESET (FDh) Operation



Identification Operations

READ ID (90h)

The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by a 00h address cycle, the target returns 8 bytes, most of which is an identifier code that includes the manufacturer ID, device configuration, and part-specific information.

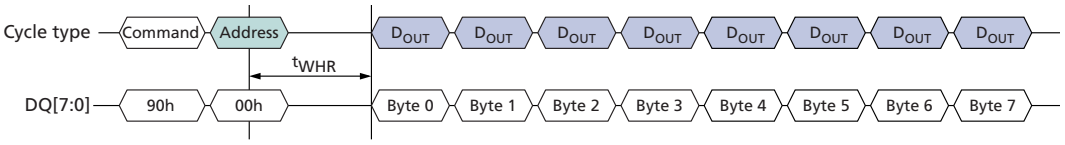
When the 90h command is followed by a 20h address cycle, the target returns 6 bytes of data beginning with the 4-byte ONFI identifier code ('O' = 4Fh, 'N' = 4Eh, 'F' = 46h, 'I' = 49h).

When the 90h command is followed by a 40h address cycle, the target returns 6 bytes of data beginning with the 5-byte JEDEC identifier code ('J' = 4Ah, 'E' = 45h, 'D' = 44h, 'E' = 45h, 'C' = 43h).

After the 90h and address cycle are written to the target, the host enables data output mode to read the identifier information. One data byte is output per rising edge of DQS when ALE and CLE are LOW; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS.

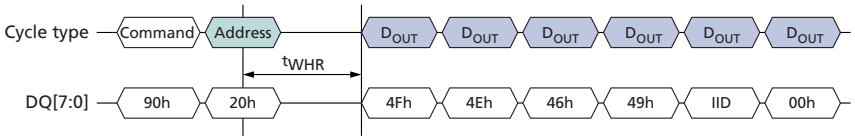
If host issues READ ID (90h) command during a program data load sequence, first the data load sequence must be closed and internal pipeline flushed with an 11h command prior to issuing the command.

Figure 45: READ ID (90h) with 00h Address Operation



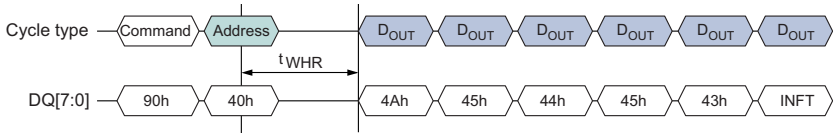
Note: 1. See the READ ID Parameter tables for byte definitions.

Figure 46: READ ID (90h) with 20h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.

Figure 47: READ ID (90h) with 40h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.

READ ID Parameter Tables

Table 19: Read ID Parameters for Address 00h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
MT29F512G08EBLEE	2Ch	C3h	08h	32h	EAh	30h	00h	00h
MT29F1T08EELEE	2Ch	C3h	08h	32h	EAh	30h	00h	00h
MT29F2T08EMLEE	2Ch	C3h	08h	32h	EAh	30h	00h	00h
MT29F4T08EULEE	2Ch	D3h	89h	32h	EAh	30h	00h	00h
MT29F8T08EWLEE	2Ch	E3h	8Ah	32h	EAh	30h	00h	00h

Notes: 1. h = hexadecimal.

Table 20: Read ID Parameters for Address 20h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
MT29F512G08EBLEE	4Fh	4Eh	46h	49h	01h
MT29F1T08EELEE	4Fh	4Eh	46h	49h	01h
MT29F2T08EMLEE	4Fh	4Eh	46h	49h	01h
MT29F4T08EULEE	4Fh	4Eh	46h	49h	01h
MT29F8T08EWLEE	4Fh	4Eh	46h	49h	01h

Notes: 1. h = hexadecimal.

Table 21: Read ID Parameters for Address 40h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
NV-DDR3	4Ah	45h	44h	45h	43h	10h

Notes: 1. h = hexadecimal.

READ PARAMETER PAGE (ECh)

The READ PARAMETER PAGE (ECh) command is used to read the ONFI or JEDEC parameter page programmed into the target. This command shall be issued only when all LUNs are in IDLE.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When the ECh command is followed by an 00h or 40h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. Use of the READ STATUS ENHANCED (78h) command and FIXED ADDRESS READ STATUS ENHANCED (71h) is prohibited while the target is busy and during data output.

After ^{t}R completes, the host enables data output mode to read the parameter page. One data byte is output for each rising or falling edge of DQS.

All data from READ PARAMETER PAGE must be output before issuing any command other than READ STATUS (70h), which requires READ MODE (00h) or CHANGE READ COLUMN (05h-E0h) command to re-enable data output. If data output is interrupted, the READ PARAMETER PAGE (ECh) command needs to be reissued to the NAND.

A minimum of three copies of the parameter page are stored in the device. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the location of data output. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h or 00h-05h-E0h) command is prohibited.

The READ PARAMETER PAGE (ECh) output data can be used by the host to configure its internal settings to properly use the NAND Flash device. Parameter page data is static per part, however the value can be changed through the product cycle of NAND Flash. The host should interpret the data and configure itself accordingly.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. Parameter pages returned by the target may have invalid CRC values; however, bit-wise majority may be used to recover the contents of the parameter page. The host may use bit-wise majority or other techniques to recover the contents of the parameter page from the parameter page copies present.

Figure 48: READ PARAMETER (ECh) with 00h Address Operation for ONFI

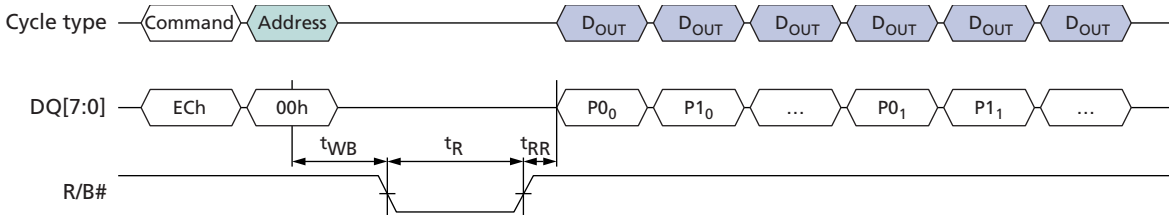
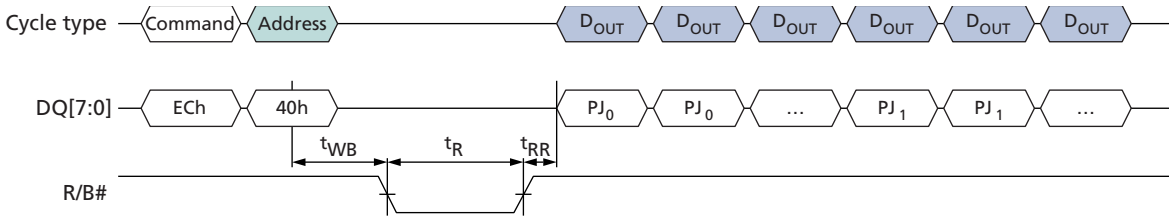


Figure 49: READ PARAMETER (ECh) with 40h Address Operation for JEDEC



Parameter Page Data Structure Tables

Table 22: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
Revision information and features block			
0–3	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	–	4Fh, 4Eh, 46h, 49h
4–5	Revision number Bit[15:12]: Reserved (0) Bit 11: 1 = supports ONFI version 4.2 Bit 10: 1 = supports ONFI version 4.1 Bit 9: 1 = supports ONFI version 4.0 Bit 8: 1 = supports ONFI version 3.2 Bit 7: 1 = supports ONFI version 3.1 Bit 6: 1 = supports ONFI version 3.0 Bit 5: 1 = supports ONFI version 2.3 Bit 4: 1 = supports ONFI version 2.2 Bit 3: 1 = supports ONFI verion 2.1 Bit 2: 1 = supports ONFI version 2.0 Bit 1: 1 = supports ONFI version 1.0 Bit 0: Reserved (0)	–	00h, 08h
6–7	Features supported Bit15: 1 = supports Package Electrical Specification Bit 14: 1 = supports ZQ calibration Bit 13: 1 = supports NV-DDR3 Bit 12: 1 = supports external V_{PP} Bit 11: 1 = supports Volume addressing Bit 10: 1 = supports NV-DDR2 interface Bit 9: 1 = Reserved Bit 8: 1 = supports program page register clear enhancement Bit 7: 1 = supports extended parameter page Bit 6: 1 = supports interleaved (multi-plane) read operations Bit 5: 1 = supports NV-DDR interface Bit 4: 1 = supports odd-to-even page copyback Bit 3: 1 = supports interleaved (multi-plane) program and erase operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit 0: 1 = supports 16-bit data bus width	MT29F512G08EBLEEJ4 MT29F1T08EELEEJ4 MT29F2T08EMLEEJ4 MT29F4T08EULEEM4 MT29F8T08EWLEEM5	D8h, F9h DAh, F9h

Table 22: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
8–9	Optional commands supported Bit[15:14]: Reserved (0) Bit 13: 1 = supports ZQ calibration (Long and Short) Bit 12: 1 = supports GET/SET Features by LUN Bit 11: 1 = supports ODT CONFIGURE Bit 10: 1 = supports VOLUME SELECT Bit 9: 1 = supports RESET LUN Bit 8: 1 = supports small data move Bit 7: 1 = supports CHANGE ROW ADDRESS Bit 6: 1 = supports CHANGE READ COLUMN ENHANCED Bit 5: 1 = supports READ UNIQUE ID Bit 4: 1 = supports COPYBACK Bit 3: 1 = supports READ STATUS ENHANCED Bit 2: 1 = supports GET FEATURES and SET FEATURES Bit 1: 1 = supports read cache commands Bit 0: 1 = supports PROGRAM PAGE CACHE	–	FFh, 3Fh
10	ONFI-JEDEC JTG primary advanced command support Bit[7:4]: Reserved (0) Bit 3: 1 = supports ERASE BLOCK MULTI-PLANE Bit 2: 1 = supports COPYBACK PROGRAM MULTI-PLANE Bit 1: 1 = supports PROGRAM PAGE MULTI-PLANE Bit 0: 1 = supports CHANGE READ COLUMN	–	0Fh
11	Training commands supported Bit[7:5]: Reserved (0) Bit 4: 1 = supports Write Rx DQ training Bit 3: 1 = supports Write Tx DQ training Bit 2: 1 = supports Read DQ training Bit 1: 1 = supports Implicit (command based) DCC training Bit 0: 1 = supports Explicit DCC training	–	0Dh
12–13	Extended parameter page length	–	03h, 00h
14	Number of parameter pages	–	3Ch
15–31	Reserved (0)	–	All 00h
Manufacturer information block			
32–43	Device manufacturer (12 ASCII characters) Micron	–	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h

Table 22: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
44–63	Device model (20 ASCII characters)	MT29F512G08EBLEEJ4	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 45h, 42h, 4Ch, 45h, 45h, 4Ah, 34h, 20h, 20h
		MT29F1T08EELEEJ4	4Dh, 54h, 32h, 39h, 46h, 31h, 54h, 30h, 38h, 45h, 45h, 4Ch, 45h, 45h, 4Ah, 34h, 20h, 20h, 20h, 20h
		MT29F2T08EMLEEJ4	4Dh, 54h, 32h, 39h, 46h, 32h, 54h, 30h, 38h, 45h, 4Dh, 4Ch, 45h, 45h, 4Ah, 34h, 20h, 20h, 20h, 20h
		MT29F4T08EULEEM4	4Dh, 54h, 32h, 39h, 46h, 34h, 54h, 30h, 38h, 45h, 55h, 4Ch, 45h, 45h, 4Dh, 34h, 20h, 20h, 20h, 20h
		MT29F8T08EWLEEM5	4Dh, 54h, 32h, 39h, 46h, 38h, 54h, 30h, 38h, 45h, 57h, 4Ch, 45h, 45h, 4Dh, 35h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	–	2Ch

Table 22: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
65–66	Date code	–	00h, 00h
67–79	Reserved (0)	–	All 00h
Memory organization block			
80–83	Number of data bytes per page	–	00h, 40h, 00h, 00h
84–85	Number of spare bytes per page	–	B0h, 07h
86–91	Reserved (0)	–	All 00h
92–95	Number of pages per block	–	40h, 08h, 00h, 00h
96–99	Number of blocks per LUN	–	B0h, 08h, 00h, 00h
100	Number of LUNs per chip enable	MT29F512G08EBLEEJ4	01h
		MT29F1T08EELEEJ4	01h
		MT29F2T08EMLEEJ4	01h
		MT29F4T08EULEEM4	02h
		MT29F8T08EWLEEM5	04h
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	24h
102	Number of bits per cell	–	03h
103–104	Bad blocks maximum per LUN	–	78h, 00h
105–106	Block endurance	–	03h, 03h
107	Guaranteed valid blocks at beginning of target	–	01h
108–109	Block endurance for guaranteed valid blocks	–	00h, 00h
110	Number of programs per page	–	01h
111	Reserved (0)	–	00h
112	Number of bits ECC correctability	–	FFh
113	Number of Bits to Address the Number of Planes in the Device Bit[7:4]: Reserved (0) Bit[3:0]: Number of Plane Select Bits	–	02h
114	Interleaved operation attributes Bit[7:6]: Reserved (0) Bit 5: Reserved Bit 4: 1 = supports read cache Bit 3: Address restrictions for cache operations Bit 2: 1 = supports program cache Bit 1: 1 = no block address restrictions Bit 0: Overlapped/concurrent interleaving support	–	1Eh
115–127	Reserved (0)	–	All 00h
Electrical parameters block			

Table 22: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
128	I/O pad capacitance per chip enable	MT29F512G08EBLEEJ4	02h
		MT29F1T08EELEEJ4	02h
		MT29F2T08EMLEEJ4	02h
		MT29F4T08EULEEM4	04h
		MT29F8T08EWLEEM5	08h
129–130	Asynchronous timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	00h, 00h
131–132	Reserved (0)	–	All 00h
133–134	^{t}PROG Maximum PROGRAM PAGE time (µs)	–	D3h, 08h
135–136	^{t}BERS Maximum BLOCK ERASE time (µs)	–	20h, 4Eh
137–138	^{t}R Maximum PAGE READ time (µs)	–	43h, 00h
139–140	^{t}CCS Minimum change column setup time (ns)	–	90h, 01h
141	NV-DDR timing mode support Bit[7:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	–	00h
142	NV-DDR2 timing mode support Bit 7: 1 = supports timing mode 7 Bit 6: 1 = supports timing mode 6 Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	–	00h
143	NV-DDR/NV-DDR2 features Bit[7:4]: Reserved (0) Bit 3: 0 = device does not require V_{PP} enablement sequence Bit 2: 1 = devices support CLK stopped for data input Bit 1: 1 = typical capacitance values present Bit 0: 0 = use ^{t}CAD MIN value	–	00h

Table 22: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
144–145	CLK input pin capacitance, typical	MT29F512G08EBLEEJ4	00h, 00h
		MT29F1T08EELEEJ4	00h, 00h
		MT29F2T08EMLEEJ4	00h, 00h
		MT29F4T08EULEEM4	00h, 00h
		MT29F8T08EWLEEM5	00h, 00h
146–147	I/O pad capacitance, typical	MT29F512G08EBLEEJ4	0Bh, 00h
		MT29F1T08EELEEJ4	0Bh, 00h
		MT29F2T08EMLEEJ4	0Bh, 00h
		MT29F4T08EULEEM4	16h, 00h
		MT29F8T08EWLEEM5	2Ch, 00h
148–149	Input capacitance, typical	MT29F512G08EBLEEJ4	28h, 00h
		MT29F1T08EELEEJ4	28h, 00h
		MT29F2T08EMLEEJ4	28h, 00h
		MT29F4T08EULEEM4	41h, 00h
		MT29F8T08EWLEEM5	69h, 00h
150	Input pin capacitance, maximum	MT29F512G08EBLEEJ4	05h
		MT29F1T08EELEEJ4	05h
		MT29F2T08EMLEEJ4	05h
		MT29F4T08EULEEM4	08h
		MT29F8T08EWLEEM5	0Dh
151	Driver strength support. If the device supports NV-DDR3 data interface, then one and only one of bit 0, bit 3, and bit 4 shall be set. If bit 0, bit 3, and bit 4 are all cleared to zero, then the driver strength at power-on is undefined. Bit[7:5]: Reserved (0) Bit 4: 1 = supports 35 Ohm, 37.5 Ohm, and 50 Ohm drive strength (Default is 35 Ohm) Bit 3: 1 = supports 37.5 Ohm and 50 Ohm drive strength (Default is 37.5 Ohm) Bit 2: 1 = supports 18 Ohm driver strength Bit 1: 1 = supports 25 Ohm driver strength Bit 0: 1 = supports 35 Ohm and 50 Ohm driver strength (Default is 35 Ohm)	–	08h
152–153	^{t}R maximum interleaved (multi-plane) page read time (µs)	–	43h, 00h
154-155	^{t}ADL program page register clear enhancement value (ns)	–	96h, 00h
156–157	Reserved (0)	–	All 00h

Table 22: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
158	NV-DDR2/3 features Bit[7:6]: Reserved (0) Bit 5: 0 = external V_{REFQ} not required for >= 200MT/s Bit 4: 1 = supports differential signaling for DQS Bit 3: 1 = supports differential signaling for RE# Bit 2: 1 = supports ODT value of 30 ohms Bit 1: 1 = supports matrix termination ODT Bit 0: 1 = supports self-termination ODT	–	1Bh
159	NV-DDR2/3 warmup cycles Bit[7:4]: Data input warmup cycles support Bit[3:0]: Data output warmup cycles support	–	44h
160–161	NV-DDR3 timing mode support Bit [15:13]: Reserved (0) Bit 12: 1 = supports timing mode 15 Bit 11: 1 = supports timing mode 14 Bit 10: 1 = supports timing mode 13 Bit 9: 1 = supports timing mode 12 Bit 8: 1 = supports timing mode 11 Bit 7: 1 = supports timing mode 10 Bit 6: 1 = supports timing mode 9 Bit 5: 1 = supports timing mode 8 Bit 4: 1 = supports timing mode 7 Bit 3: 1 = supports timing mode 6 Bit 2: 1 = supports timing mode 5 Bit 1: 1 = supports timing mode 4 Bit 0: 1 = supports timing mode 0 to 3	–	FFh, 1Fh
162	NV-DDR2 timing mode support Bit [7:3]: Reserved (0) Bit 2: 1 = supports timing mode 10 Bit 1: 1 = supports timing mode 9 Bit 0: 1 = supports timing mode 8	–	00h
163	Reserved (0)	–	00h
Vendor block			
164–165	Vendor-specific revision number	–	01h, 00h
166	TWO-PLANE PAGE READ support Bit[7:1]: Reserved (0) Bit 0: 1 = Support for TWO-PLANE PAGE READ	–	01h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support Micron-specific read cache function	–	00h
168	READ UNIQUE ID support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support Micron-specific READ UNIQUE ID	–	00h
169	Programmable DQ output impedance support Bit[7:1]: Reserved (0) Bit 0: 0 = No support for programmable DQ output impedance by B8h command	–	00h

Table 22: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
170	Number of programmable DQ output impedance settings Bit[7:3]: Reserved (0) Bit [2:0] = Number of programmable DQ output impedance settings	–	02h
171	Programmable DQ output impedance feature address Bit[7:0] = Programmable DQ output impedance feature address	–	10h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 1 = Support programmable R/B# pull-down strength	–	01h
173	Programmable R/B# pull-down strength feature address Bit[7:0] = Feature address used with programmable R/B# pull-down strength	–	81h
174	Number of programmable R/B# pull-down strength settings Bit[7:3]: Reserved (0) Bit[2:0] = Number of programmable R/B# pull-down strength settings	–	04h
175	OTP mode support Bit[7:2]: Reserved (0) Bit 1: 1 = Supports Get/Set Features command set Bit 0: 0 = Does not support A5h/A0h/AFh OTP command set	–	02h
176	OTP page start Bit[7:0] = Page where OTP page space begins	–	04h
177	OTP DATA PROTECT address Bit[7:0] = Page address to use when issuing OTP DATA PROTECT command	–	01h
178	Number of OTP pages Bit[15:5]: Reserved (0) Bit[4:0] = Number of OTP pages	–	1Ch
179	OTP Feature Address	–	90h
180	Read Retry Options Bit[7:5]: Reserved (0) Bit[4:0] = Number of Read Retry options supported	–	00h
181–184	Read Retry Options available. A value of '1' in a bit position shows that Read Retry option is available for use. A value of '0' in a bit position shows that Read Retry option is not available for use. For example, the binary value of '37h, 00h, 00h, 00h' would represent that Read Retry options 0, 1, 2, 4, and 5 are available which would correspond to Read Retry input option selections of 00h, 01h, 02h, 04h, and 05h. It furthermore would show that Read Retry options 3, 6, and 7 to 32 which would correspond to Read Retry input option selections 03h, 06h, 07h to 20h, are not available.	–	00h, 00h, 00h, 00h
185	LDPC ECC requirement Bit[7:1]: Reserved (0) Bit 0: 1 = LDPC ECC is required		01h

Table 22: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
186	Address Cycle Read Retry (ACRR) enablement Feature Address	–	96h
187-188	Address Cycle Read Retry (ACRR) subfeature position for enablement and subfeature bit position for enablement Bits[15:12]: Reserved (0) Bits[11:8]: Subfeature for enablement Bits[7:0]: Subfeature bit position for enablement	–	01h, 04h
189-192	Address Cycle Read Retry (ACRR) Options available. A value of '1' in a bit position shows that ACRR option is available for use. A value of 'o' in a bit position shows that ACRR option is not available for use.	–	FFh, 00h, 00h, 00h
193-194	SLC mode support Bits[15:3]: Reserved (0) Bit[2] 1 = Factory Reserved Setting Bit[1:0] 11 = Op-Code 3Bh supported only Bit[1:0]10 = Op-Codes 3Bh/3Ch supported only Bit[1:0] 01 = Feature Address 91h and Op-Codes 3Bh/3Ch supported Bit[1:0] 00 = Feature Address 91h and Op-Codes DAh/DFh supported	–	03h, 00h
195-196	Plane Select LSB Bit Position in the Row Address Field	–	0Ch, 00h
197–249	Reserved (0)	–	All 00h
250–252	Designator Bytes 1 to 3 (ASCII characters) Byte 250 = Designator Byte 1, "R", Byte 251 = Designator Byte 2 Byte 252 = Designator Byte 3	–	52h, 00h, 00h
253	Parameter page revision	–	01h
254–255	Integrity CRC	MT29F512G08EBLEEJ4	08h, 47h
		MT29F1T08EELEEJ4	B3h, 8Fh
		MT29F2T08EMLEEJ4	03h, 0Dh
		MT29F4T08EULEEM4	96h, B2h
		MT29F8T08EWLEEM5	EAh, 3Eh
Redundant parameter pages			
256–511	Value of bytes 0–255	–	See bytes 0–255
512–767	Value of bytes 0–255	–	See bytes 0–255
...	...	–	...
15,104–15,359	Value of bytes 0–255	–	See bytes 0–255
Extended parameter pages			
15,360–15,361	Extended parameter page Integrity CRC	–	A6h, 65h

Table 22: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
15,362–15,365	Extended parameter page signature Byte 0: 45h, "E" Byte 1: 50h, "P" Byte 2: 50h, "P" Byte 3: 53h, "S"	–	45h, 50h, 50h, 53h
15,366–15,375	Reserved (0)	–	All 00h
15,376	Section 0 type	–	02h
15,377	Section 0 length	–	01h
15,378–15,391	Reserved (0)	–	All 00h
15,392	Number of bits ECC correctability	–	9Bh
15,393	ECC codeword size	–	0Bh
15,394–15,395	Bad blocks maximum per LUN	–	78h, 00h
15,396–15,397	Block endurance	–	03h, 03h
15,398–15,407	Reserved (0)	–	All 00h
Redundant extended parameter pages			
15,408–15,455	Value of bytes 15,360–15,407	–	See bytes 15,360–15,407
15,456–15,503	Value of bytes 15,360–15,407	–	See bytes 15,360–15,407
...	...	–	...
18,192–18,239	Value of bytes 15,360–15,407	–	See bytes 15,360–15,407
18,240 to end of page	Reserved (FFh)	–	All FFh

Table 23: JEDEC Parameter Page Definition

Byte	Description	Device	Values
Revision Information and Features Block			
0–3	Parameter page signature Byte 0: 4Ah, "J" Byte 1: 45h, "E" Byte 2: 53h, "S" Byte 3: 44h, "D"	–	4Ah, 45h, 53h, 44h
4–5	Revision number Bit[15:3]: Reserved (0) Bit 2: 1 = supports JEDEC version 1.0 and standard revision 1.0 Bit 1: 1 = supports vendor specific parameter page Bit 0: Reserved (0)	–	06h, 00h

Table 23: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
6–7	Features supported Bit[15:10]: Reserved (0) Bit 9: 1 = supports changing pin function between WP# and ODT# Bit 8: 1 = supports program page register clear enhancement Bit 7: 1 = supports external V_{PP} Bit 6: 1 = supports Toggle Mode DDR Bit 5: 1 = supports Synchronous DDR Bit 4: 1 = supports multi-plane read operations Bit 3: 1 = supports multi-plane program and erase operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit 0: 1 = supports 16-bit data bus width	MT29F512G08EBLEEJ4	98h, 01h
		MT29F1T08EELEEJ4	
		MT29F2T08EMLEEJ4	
		MT29F4T08EULEEM4	9Ah, 01h
		MT29F8T08EWLEEM5	9Ah, 01h
8–10	Features supported Bit[23:11]: Reserved (0) Bit 10: 1 = supports Synchronous Reset Bit 9: 1 = supports Reset LUN (Primary) Bit 8: 1 = supports Small Data Move Bit 7: 1 = supports Multi-plane Copyback Program (Primary) Bit 6: 1 = supports Random Data Out (Primary) Bit 5: 1 = supports Read Unique ID Bit 4: 1 = supports Copyback Bit 3: 1 = supports Read Status Enhanced (Primary) Bit 2: 1 = supports Get Features and Set Features Bit 1: 1 = supports Read Cache commands Bit 0: 1 = supports Page Cache Program command	–	FFh, 03h, 00h
11–12	Secondary commands supported Bit[15:8]: Reserved (0) Bit 7: 1 = supports secondary Read Status Enhanced Bit 6: 1 = supports secondary Multi-plane Block Erase Bit 5: 1 = supports secondary Multi-plane Copyback Program Bit 4: 1 = supports secondary Multi-plane Program Bit 3: 1 = supports secondary Random Data Out Bit 2: 1 = supports secondary Multi-plane Copyback Read Bit 1: 1 = supports secondary Multi-plane Read Cache Random Bit 0: 1 = supports secondary Multi-plane Read	–	58h, 00h
13	Number of Parameter Pages	–	23h
14–31	Reserved (0)	–	All 00h
Manufacturer information block			
32–43	Device manufacturer (12 ASCII characters) Micron	–	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h

Table 23: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
44–63	Device model (20 ASCII characters)	MT29F512G08EBLEEJ4	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 45h, 42h, 4Ch, 45h, 45h, 4Ah, 34h, 20h, 20h
		MT29F1T08EELEEJ4	4Dh, 54h, 32h, 39h, 46h, 31h, 54h, 30h, 38h, 45h, 45h, 4Ch, 45h, 45h, 4Ah, 34h, 20h, 20h, 20h, 20h
		MT29F2T08EMLEEJ4	4Dh, 54h, 32h, 39h, 46h, 32h, 54h, 30h, 38h, 45h, 4Dh, 4Ch, 45h, 45h, 4Ah, 34h, 20h, 20h, 20h, 20h
		MT29F4T08EULEEM4	4Dh, 54h, 32h, 39h, 46h, 34h, 54h, 30h, 38h, 45h, 55h, 4Ch, 45h, 45h, 4Dh, 34h, 20h, 20h, 20h, 20h
		MT29F8T08EWLEEM5	4Dh, 54h, 32h, 39h, 46h, 38h, 54h, 30h, 38h, 45h, 57h, 4Ch, 45h, 45h, 4Dh, 35h, 20h, 20h, 20h, 20h
64–69	JEDEC manufacturer ID	–	2Ch, 00h, 00h, 00h, 00h, 00h
70–71	Reserved (0)	–	All 00h
72–79	Reserved (0)	–	All 00h
Memory organization block			
80–83	Number of data bytes per page	–	00h, 40h, 00h, 00h
84–85	Number of spare bytes per page	–	B0h, 07h
86–89	Number of data bytes per partial page	–	00h, 08h, 00h, 00h
90–91	Number of spare bytes per partial page	–	F6h, 00h
92–95	Number of pages per block	–	40h, 08h, 00h, 00h

Table 23: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
96–99	Number of blocks per LUN	–	B0h, 08h, 00h, 00h
100	Number of LUNs per chip enable	MT29F512G08EBLEEJ4	01h
		MT29F1T08EELEEJ4	01h
		MT29F2T08EMLEEJ4	01h
		MT29F4T08EULEEM4	02h
		MT29F8T08EWLEEM5	04h
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	24h
102	Number of bits per cell	–	03h
103	Number of programs per page	–	01h
104	Multi-plane operation addressing Bit[7:4]: Reserved (0) Bit[3:0]: Number of plane address bits	–	02h
105	Multi-plane operation attributes Bit[7:3]: Reserved (0) Bit 2: 1 = Read cache operations supported Bit 1: 1 = Program cache operations supported Bit 0: 1 = Address restrictions for cache operations	–	07h
106-143	Reserved (0)	–	All 00h
Electrical parameters block			
144–145	Asynchronous SDR speed grade support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	00h, 00h
146–147	Synchronous DDR2 speed grade support Bit[15:11]: Reserved (0) Bit 10: 1 = supports timing mode 10 Bit 9: 1 = supports timing mode 9 Bit 8: 1 = supports timing mode 8 Bit 7: 1 = supports timing mode 7 Bit 6: 1 = supports timing mode 6 Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	00h, 00h

Table 23: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
148–149	Synchronous DDR speed grade support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	00h, 00h
150	Asynchronous SDR features Bit[7:0]: Reserved (0)	–	00h
151	Reserved (0)	–	00h
152	Synchronous DDR features Bit[7:2]: Reserved (0) Bit 1: 1 = devices leave CLK running for data input Bit 0: 0 = use ^{t}CAD MIN value	–	00h
153–154	^{t}PROG Maximum PROGRAM PAGE time (µs)	–	D3h, 08h
155–156	^{t}BERS Maximum BLOCK ERASE time (µs)	–	20h, 4Eh
157–158	^{t}R Maximum PAGE READ time (µs)	–	43h, 00h
159–160	^{t}R Maximum Multi-PLANE PAGE READ time (µs)	–	43h, 00h
161–162	^{t}CCS Minimum change column setup time (ns)	–	90h, 01h
163–164	I/O pad capacitance, typical	MT29F512G08EBLEEJ4	0Bh, 00h
		MT29F1T08EELEEJ4	0Bh, 00h
		MT29F2T08EMLEEJ4	0Bh, 00h
		MT29F4T08EULEEM4	16h, 00h
		MT29F8T08EWLEEM5	2Ch, 00h
165–166	Input capacitance, typical	MT29F512G08EBLEEJ4	28h, 00h
		MT29F1T08EELEEJ4	28h, 00h
		MT29F2T08EMLEEJ4	28h, 00h
		MT29F4T08EULEEM4	41h, 00h
		MT29F8T08EWLEEM5	69h, 00h
167–168	CLK input pin capacitance, typical	MT29F512G08EBLEEJ4	00h, 00h
		MT29F1T08EELEEJ4	00h, 00h
		MT29F2T08EMLEEJ4	00h, 00h
		MT29F4T08EULEEM4	00h, 00h
		MT29F8T08EWLEEM5	00h, 00h

Table 23: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
169	Driver strength support. If the device supports NV-DDR, NV-DDR2, or NV-DDR3 data interface, then one and only one of bit 0, bit 3, and bit 4 shall be set. If bit 0, bit 3, and bit 4 are all cleared to zero, then the driver strength at power-on is undefined. Bit[7:5]: Reserved (0) Bit 4: 1 = supports 35 Ohm, 37.5 Ohm, and 50 Ohm drive strength (Default is 35 Ohm) Bit 3: 1 = supports 37.5 Ohm and 50 Ohm drive strength (Default is 37.5 Ohm) Bit 2: 1 = supports 18 Ohm driver strength Bit 1: 1 = supports 25 Ohm driver strength Bit 0: 1 = supports 35 Ohm and 50 Ohm driver strength (Default is 3 Ohm)	–	08h
170–171	^{t}ADL program page register clear enhancement value (ns)	–	96h, 00h
172-173	Synchronous DDR3 speed grade support Bit[15:13]: Reserved (0) Bit 12: 1 = supports timing mode 12 Bit 11: 1 = supports timing mode 11 Bit 10: 1 = supports timing mode 10 Bit 9: 1 = supports timing mode 9 Bit 8: 1 = supports timing mode 8 Bit 7: 1 = supports timing mode 7 Bit 6: 1 = supports timing mode 6 Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	FFh, 1Fh
174–207	Reserved (0)	–	All 00h
ECC and endurance block			
208	Guaranteed valid blocks at beginning of target	–	01h
209–210	Block endurance for guaranteed valid blocks	–	00h, 00h
211	Number of bits ECC correctability	–	9Bh
212	ECC codeword size	–	0Bh
213–214	Bad blocks maximum per LUN	–	78h, 00h
215–216	Block endurance	–	03h, 03h
217–218	Reserved (0)	–	All 00h
219–271	Reserved (0)	–	All 00h
Reserved			
272–419	Reserved (0)	–	All 00h
Vendor specific block			
420–421	Vendor-specific revision number	–	01h, 00h

Table 23: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
422	Read Retry Options Bit[7:5]: Reserved (0) Bit[4:0] = Number of Read Retry options supported	–	00h
423–426	Read Retry Options available. A value of '1' in a bit position shows that Read Retry option is available for use. A value of '0' in a bit position shows that Read Retry option is not available for use. For example, the binary value of '37h, 00h, 00h, 00h' would represent that Read Retry options 0, 1, 2, 4, and 5 are available which would correspond to Read Retry input option selections of 00h, 01h, 02h, 04h, and 05h. It furthermore would show that Read Retry options 3, 6, and 7 to 32 which would correspond to Read Retry input option selections 03h, 06h, 07h to 20h, are not available.	–	00h, 00h, 00h, 00h
427–429	Designator Bytes 1 to 3 (ASCII characters) Byte 427 = Designator Byte 1, "R", Byte 428 = Designator Byte 2 Byte 429 = Designator Byte 3	–	52h, 00h, 00h
430	LDPC ECC requirement Bit[7:1]: Reserved (0) Bit 0: 1 = LDPC ECC is required		01h
431	Address Cycle Read Retry (ACRR) enablement Feature Address	–	96h
432-433	Address Cycle Read Retry (ACRR) subfeature position for enablement and subfeature bit position for enablement Bits[15:12]: Reserved (0) Bits[11:8]: Subfeature for enablement Bits[7:0]: Subfeature bit position for enablement	–	01h, 04h
434-437	Address Cycle Read Retry (ACRR) Options available. A value of '1' in a bit position shows that ACRR option is available for use. A value of '0' in a bit position shows that ACRR option is not available.	–	FFh, 00h, 00h, 00h
438-439	SLC mode support Bits[15:3]: Reserved (0) Bit[2] 1 = Factory Reserved Setting Bit[1:0] 11 = Op-Code 3Bh supported only Bit[1:0]10 = Op-Codes 3Bh/3Ch supported only Bit[1:0] 01 = Feature Address 91h and Op-Codes 3Bh/3Ch supported Bit[1:0] 00 = Feature Address 91h and Op-Codes DAh/DFh supported	–	03h, 00h
440–509	Reserved (0)	–	All 00h
CRC for Parameter Page			
510–511	Integrity CRC	MT29F512G08EBLEEJ4	2Bh, 6Bh
		MT29F1T08EELEEJ4	E6h, FBh
		MT29F2T08EMLEEJ4	16h, 69h
		MT29F4T08EULEEM4	41h, EAh
		MT29F8T08EWLEEM5	3Dh, CCh

Table 23: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
Redundant JEDEC Parameter Pages			
512–1023	See byte values 0–511	–	See bytes 0–511
1024–1535	See byte values 0–511	–	See bytes 0–511
...	...	–	...
17,408–17,919	See byte values 0–511	–	See bytes 0–511
17,920 to end of page	Reserved (FFh)	–	All FFh

Notes: 1. h = hexadecimal.

READ UNIQUE ID (EDh)

The READ UNIQUE ID (EDh) command is used to read a unique identifier programmed into the target. This command shall be issued only when all LUNs are in IDLE.

Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

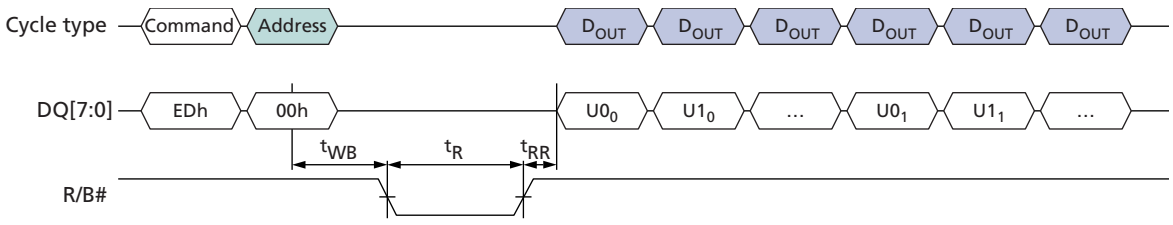
When the EDh command is followed by a 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

After ^{t}R completes, the host enables data output mode to read the unique ID. For the NV-DDR3 interface, two data bytes are output per DQS toggle, one byte for each rising or falling edge of DQS.

All data from READ UNIQUE ID must be output before issuing any command other than READ STATUS (70h), which requires READ MODE (00h) or CHANGE READ COLUMN (05h-E0h) command to re-enable data output. If data output is interrupted, the READ UNIQUE ID (EDh) command needs to be reissued to the NAND.

Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the data output location. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h) command is prohibited.

Figure 50: READ UNIQUE ID (EDh) Operation



Configuration Operations

The SET FEATURES (EFh) and GET FEATURES (EEh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which subfeature parameters will be read or modified. Each feature address (in the 00h to FFh range) is defined in Feature Address Definitions table. The SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command writes subfeature parameters (P1-P4) to the specified feature address. The GET FEATURES (EEh) or GET FEATURES by LUN (D4h) command reads the subfeature parameters (P1-P4) at the specified feature address.

Unless otherwise specified, the values of the feature addresses do not change when RESET (FAh, FFh) is issued by the host. A HARD RESET (FDh) command will reset all feature addresses to their default values for the target LUN. A HARD RESET (FDh) command will not undo any previously set Electronic Mirroring, CE# Pin Reduction, or Volume Addressing assignments that were performed prior to the HARD RESET (FDh) command.

Table 24: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h	NV-DDR3 configuration
03h–0Fh	Reserved
10h	Programmable output drive strength
11h–1Fh	Reserved
20h	DCC Training and Write DQ Training (Tx Side)
21h-2Fh	Reserved
30h	V_{PP} configuration
31h–57h	Reserved
58h	Volume configuration
59h–7Eh	Reserved
7Fh	Manual Dynamic Word Line Start Voltage
80h	Reserved
81h	Programmable RB# pull-down strength
82h	Reserved
83h	Internal/External ZQ Calibration Switching
84h	Clear Extended Status Register
85h	Reserved
86h	Read Offset Values Reset
87h	Sleep Lite
88h-8Fh	Reserved
90h	Array operation mode
91h–95h	Reserved
96h	Auto Read Calibration & Address Cycle Read Retry
97h–9Fh	Reserved

Table 24: Feature Address Definitions (Continued)

Feature Address	Definition
A0h-ABh	Read Offset Controls for RL1_2bpc, RL2_2bpc, RL3_2bpc, RSLC, RL1_3bpc, RL2_3bpc, RL3_3bpc, RL4_3bpc, RL5_3bpc, RL6_3bpc, RL7_3bpc (see READ OFFSET PREFIX (2Eh) Command section)
ACh-B0h	Reserved
B1h–B4h	SBSBR negative and positive offset levels to support A5h-ABh Levels (see Single Bit Soft Bit Read Operations section)
B5h–D9h	Reserved
DAh	Thermal Alert Control
DBh-E0h	Reserved
E1h-E3h	SBSBR negative and positive offset levels to support A0h-A4h Levels (see Single Bit Soft Bit Read Operations section)
E4h–E6h	Reserved
E7h	Temperature sensor
E8h-FFh	Reserved

Feature Address Register Bit Usage Restrictions

For all feature address register bit definition tables in this specification, the following usage restrictions shall apply:

1. Feature address bits labeled "Reserved" shall be cleared by the host to zero during SET FEATURE (EFh/D5h) commands to those bits.
2. The host shall not check the value of feature address bits labeled "Reserved" as the value of these bits in response to a GET FEATURE (EEh/D4h) command is not guaranteed.
3. The host shall not set feature address bit values to table options labelled "Not supported".

SET FEATURES (EFh)

The SET FEATURES (EFh) command writes the subfeature parameters (P1-P4) to the specified feature address to enable or disable target-specific features. This command shall be issued only when all LUNs are idle.

Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The EFh command is followed by a valid feature address as specified in Feature Address Definitions table. The host waits for ^{t}ADL before the subfeature parameters are input. For NV-DDR3 interface, one subfeature parameter is latched per rising edge of DQS. The data on the falling edge of DQS should be identical to the subfeature parameter input on the previous rising edge of DQS. The device is not required to wait for the repeated data byte before beginning internal actions.

After all four subfeature parameters are input, the target goes busy for ^{t}FEAT. It is not allowed to input more than four subfeature parameters. For 1 LUN per target (CE#) configurations, the READ STATUS (70h), READ STATUS ENHANCED (78h) and FIXED ADDRESS READ STATUS ENHANCED (71h) commands are allowed to monitor for command completion. For multi-LUN per target (CE#) configurations, only the READ STATUS ENHANCED (78h) and FIXED ADDRESS READ STATUS ENHANCED (71h) command are allowed to monitor for command completion. The READ STATUS ENHANCED (78h) and FIXED ADDRESS READ STATUS ENHANCED (71h) commands reflect the status of only 1 LUN in the target. To ensure command completion on all LUNs on the target, the host may either issue the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command

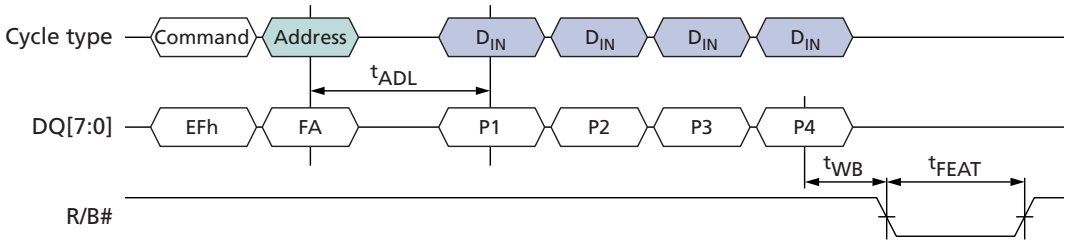
to each LUN on the target to ensure command completion on each LUN, or wait ^{t}FEAT time prior to issuing the next command.

Use of Read Status (70h/71h/78h) commands however are not allowed during the ^{t}FEAT time following a SET FEATURES (EFh/D5h) in these instances:

- After interface configurations changes via SET FEATURES (EFh/D5h) command to Feature Address 02h
- After Sleep Lite mode was enabled on a LUN via SET FEATURES (EFh/D5h) command to Feature Address 87h

If host issues SET FEATURES (EFh) command during a program data load sequence, first the data load sequence must be closed and internal pipeline flushed with an 11h command prior to issuing the command.

Figure 51: SET FEATURES (EFh) Operation



Note: 1. Feature Address registers at address less than 80h will have ^{t}FEAT < ^{t}FEAT1. Feature Address registers at address 80h and above will have ^{t}FEAT < ^{t}FEAT2. See Electrical Specifications - Array Characteristics Table for ^{t}FEAT1 and ^{t}FEAT2 spec values.

GET FEATURES (EEh)

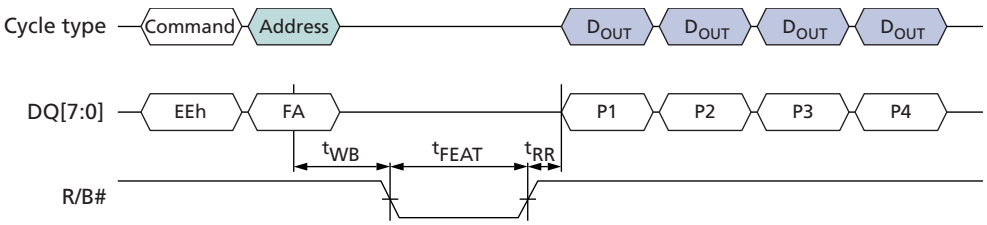
The GET FEATURES (EEh) command reads the subfeature parameters (P1-P4) from the specified feature address. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the EEh command is followed by a feature address, the target goes busy for ^{t}FEAT. For 1 LUN per target (CE#) configurations, the READ STATUS (70h), READ STATUS ENHANCED (78h) and FIXED ADDRESS READ STATUS ENHANCED (71h) commands are allowed to monitor for command completion. After command completion, in order for the host to acquire the GET FEATURE data, the READ MODE (00h) command must be used. For multi-LUN per target (CE#) configurations, the GET FEATURES by LUN (D4h) command shall be used instead. See the GET/SET FEATURES by LUN (D4h/D5h) section for details.

After ^{t}FEAT completes, the host enables data output mode to read the subfeature parameters. For NV-DDR3 interface, one subfeature parameter is output per DQS toggle on rising or falling edge of DQS.

Figure 52: GET FEATURES (EEh) Operation



Note: 1. Feature Address registers at address less than 80h will have ^{t}FEAT < ^{t}FEAT1. Feature Address registers at address 80h and above will have ^{t}FEAT < ^{t}FEAT2. See Electrical Specifications - Array Characteristics Table for ^{t}FEAT1 and ^{t}FEAT2 spec values.

GET/SET FEATURES by LUN (D4h/D5h)

The original GET FEATURES (EEh) and SET FEATURES (EFh) commands were Target (CE#) based operations that did not take into account LUN addressing. By that, setting a feature address or getting a value for a feature address for a given Target (CE#) applied to all LUNs on that Target (CE#). GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) commands have the ability to also select a LUN address gives added flexibility to set the same feature address to different values for each LUN on a Target (CE#) for more complex and versatile system solutions.

GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) operations work in the same manner as the non-LUN versions of those commands that did not take LUN addressing into account. The GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) commands both have an added LUN address cycle that follows the address cycle of the feature address which denotes the LUN to select for the operation.

Table 25: GET/SET FEATURES by LUN Operation LUN address cycle decoding

Description	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
LUN											
Bits LA0 (DQ0) and LA1 (DQ1) for LUN selection	LUN0							0	0	00b	
	LUN1							0	1	01b	
	LUN2							1	0	10b	
	LUN3							1	1	11b	
Reserved	Don't Care	-	-	-	-	-	-			-	1

Notes: 1. Can be either '1' or '0'.

GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) can be issued to any addressable LUN that is not busy (RDY = 1, ARDY = 1). Target LUN status can be determined by using the READ STATUS ENHANCED (78h) command.

If host issues SET FEATURES by LUN (D5h) command during a program data load sequence, first the data load sequence must be closed and internal pipeline flushed with an 11h command prior to issuing the command.

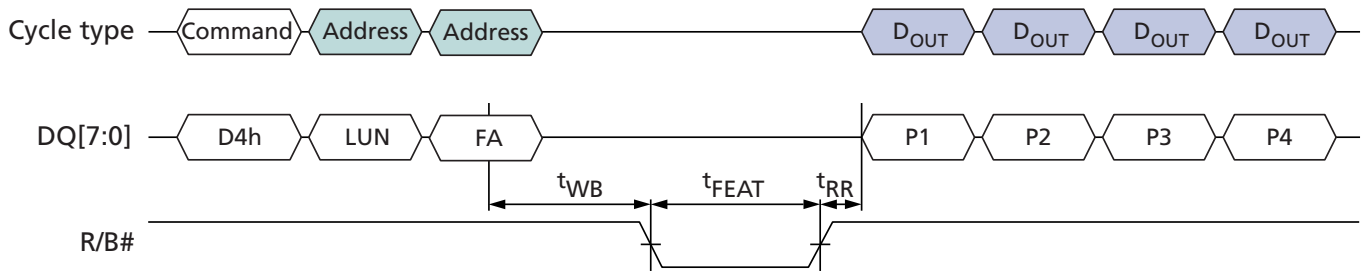
Multi-LUN Operation: For enhanced system performance during Multi-LUN operations, the following operations are allowed.

1. GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) can be issued to any addressable LUN that is not busy (RDY = 1, ARDY = 1) with the exception of GET FEATURES by LUN (D4h) and

SET FEATURES by LUN (D5h) to Feature Address 7Fh: Manual Dynamic Wordline Start Voltage, which can be issued during Program Cache with status (RDY = 1, ARDY = 0).

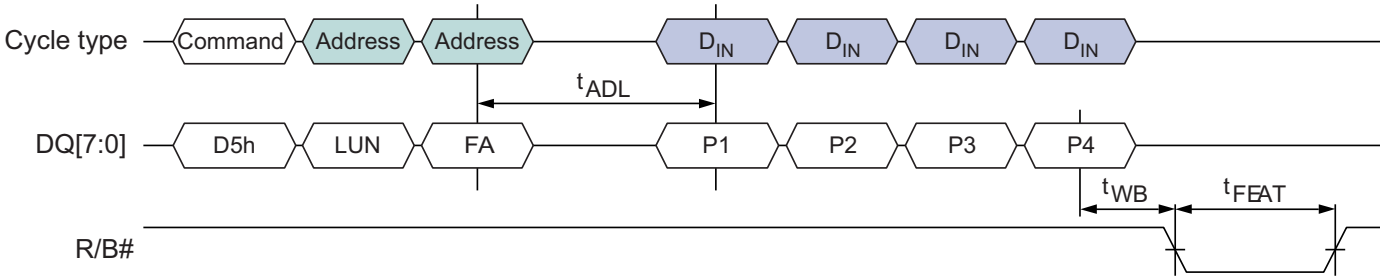
2. The host may issue a GET FEATURE by LUN (D4h) to a LUN followed by a Read/Program/Erase commands to other LUNs on the same target and then return to the first LUN to read out the feature data. To retrieve the feature data from the first LUN, the host shall issue a Read Status Enhanced (78h/71h/79h) command to the first LUN, issue the READ MODE (00h) command, and then read out the feature data from the first LUN.
   a) Issuing commands other than Read Status Enhanced (78h/71h/79h) - READ MODE (00h) to the first LUN prior to feature data readout, may prevent successful feature data readout.
   b) Issuing target level commands (ie. ERASE RESUME (D2h)/RESET (FFh)/HARD RESET (FDh) prior to feature data readout will prevent successful feature data readout from the first LUN.
3. A GET FEATURE by LUN (D4h) command may also be issued to a LUN while other LUNs on the same target are busy executing a Read/Program/Erase operation. In the case of GET FEATURE by LUN (D4h) interleaved with a Read Operation on another LUN, in order to get data from the Read Operation, the host shall issue a Read Status Enhanced (78h/71h/79h) command to the LUN that was issued the Read Operation followed by a CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command.
4. The SLC Prefix (3Bh), READ OFFSET PREFIX (2Eh), and Read Page Cache Sequential (31h) are allowed as part of the Read/Program/Erase sequence of step 2 or 3.

Figure 53: GET FEATURES by LUN (D4h) Operation



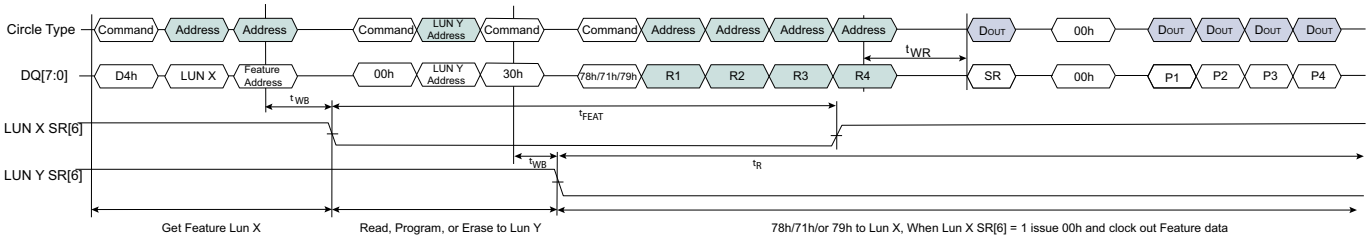
Note: 1. Feature Address registers at address less than 80h will have ^{t}FEAT < ^{t}FEAT1. Feature Address registers at address 80h and above will have ^{t}FEAT < ^{t}FEAT2. See Electrical Specifications - Array Characteristics Table for ^{t}FEAT1 and ^{t}FEAT2 spec values.

Figure 54: SET FEATURES by LUN (D5h) Operation



Note: 1. Feature Address registers at address less than 80h will have ^{t}FEAT < ^{t}FEAT1. Feature Address registers at address 80h and above will have ^{t}FEAT < ^{t}FEAT2. See Electrical Specifications - Array Characteristics Table for ^{t}FEAT1 and ^{t}FEAT2 spec values.

Figure 55: GET FEATURES by LUN (D4h) Interleaved Operation Example



Feature Address Details

Table 26: Feature Address 01h: Timing Mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Timing mode	Mode 0 (default)					0	0	0	0	x0h	1, 2
	Mode 1					0	0	0	1	x1h	
	Mode 2					0	0	1	0	x2h	
	Mode 3					0	0	1	1	x3h	
	Mode 4					0	1	0	0	x4h	
	Mode 5					0	1	0	1	x5h	
	Mode 6					0	1	1	0	x6h	
	Mode 7					0	1	1	1	x7h	
	Mode 8					1	0	0	0	x8h	
	Mode 9					1	0	0	1	x9h	
	Mode 10					1	0	1	0	xAh	
	Mode 11					1	0	1	1	xBh	
	Mode 12					1	1	0	0	xCh	
	Mode 13					1	1	0	1	xDh	
	Mode 14					1	1	1	0	xEh	
	Mode 15					1	1	1	1	xFh	
Data interface	NV-DDR3 only			1	1					11b	1, 3
Program clear	Program command clears all cache registers on a target as long as the program command is issued when RDY = 1 (default)		0							0b	
	Program command clears only the cache register of the selected plane of addressed LUN on a target.		1							1b	
Reserved		0								0b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											

Table 26: Feature Address 01h: Timing Mode (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. NV-DDR3 timing mode 0 is the default, power-on value when the NAND device is powered-on.
2. A RESET (FFh) command will change the timing mode value to its default.
3. Bit values are fixed and cannot be altered. SET FEATURE commands to Feature Address 01h, subfeature P1, must set DQ[5:4] to 11b.

Table 27: Feature Address 02h: NV-DDR3 configuration

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Voltage Reference (VEN)	External V_{REFQ} is disabled and internal voltage is used as reference for input and DQ signals (default)								0	0b	1, 6
	External V_{REFQ} is enabled and used as reference for input and DQ signals								1	1b	2
Complementary DQS (CMPD)	DQS_c signal disabled (default)							0		0b	6
	DQS_c signal enabled							1		1b	2
Complementary RE# (CMPR)	RE_c signal disabled (default)						0			0b	6
	RE_c signal enabled						1			1b	2
Reserved						0				0b	
DQ[7:0],DQS_t, DQS_c, RE_t, and RE_c ODT enable	ODT disabled (default)	0	0	0	0					0h	3, 6
	ODT enabled with R_{TT} of 150 Ohms	0	0	0	1					1h	2
	ODT enabled with R_{TT} of 75 Ohms	0	0	1	1					3h	2
	ODT enabled with R_{TT} of 50 Ohms	0	1	0	0					4h	2
	Not supported	0	0	1	0					2h	
		0	1	0	1					5h	
		0	1	1	0					6h	
		0	1	1	1					7h	
		1	X	X	X					8h-Fh	

Table 27: Feature Address 02h: NV-DDR3 configuration (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P2											
Warmup RE_t/RE_c and DQS cycles for data output	0 cycles (default)					0	0	0	0	0h	4, 6
	1 warmup cycle					0	0	0	1	1h	2
	2 warmup cycles					0	0	1	0	2h	2
	4 warmup cycles					0	0	1	1	3h	2
	4 warmup cycles					0	1	0	0	4h	2
	Not supported					0	1	0	1	5h	
						0	1	1	0	6h	
						0	1	1	1	7h	
						1	X	X	X	8h-Fh	
Warmup DQS cycles for data input	0 cycles (default)	0	0	0	0					0h	5, 6
	1 warmup cycle	0	0	0	1					1h	2
	2 warmup cycles	0	0	1	0					2h	2
	4 warmup cycles	0	0	1	1					3h	2
	4 warmup cycles	0	1	0	0					4h	2
	Not supported	0	1	0	1					5h	
		0	1	1	0					6h	
		0	1	1	1					7h	
		1	X	X	X					8h-Fh	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. If set to one, then external V_{REFQ} is used as a reference for the input and I/O signals. If cleared to zero, then internal V_{REFQ} is used as a reference for the input and I/O signals. This setting applies to input and I/O signals, including DQ[7:0], DQS_t, DQS_c, RE_t, RE_c, WE#, ALE, and CLE. CE# and WP# are CMOS signals and always use internal V_{REFQ}.

2. For NV-DDR3 interface, a RESET (FFh) or Reset LUN (FAh) command will not change the bit values of feature address 02h to their default values.
3. This field controls the on-die termination settings for the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals. R_{TT} settings may be specified separately for DQ[7:0]/DQS and the RE# signals. The DQ[7:0]/DQS may be specified separately for data input versus data output operation. Refer to the definition of the ODT CONFIGURE (E2h) command. If values are specified with the ODT CONFIGURE (E2h) command, then this field is not used. GET FEATURES (EEh) returns the previous value set in this field, regardless of the R_{TT} settings specified using ODT CONFIGURE (E2h).
4. Number of warmup cycles for and RE_t/RE_c and DQS_t/DQS_c for data output. The number of initial "dummy" RE_t/RE_c cycles at the start of data output operations for the . There are corresponding "dummy" DQS_t/DQS_c cycles to the "dummy" RE_t/RE_c cycles that the host shall ignore during data output.
5. This field indicates the number of warmup cycles of DQS that are provided for data input. These are the number of initial "dummy" DQS_t/DQS_c cycles at the start of data input operations.
6. After a SET FEATURE (EFh) or SET FEATURE by LUN (D5h) command to Feature Address 02h, the host shall bring CE# high and wait until either tFEAT time has elapsed or the R/B# signal is back high, prior to issuing any command

(including Read Status commands) to the device. The new configuration settings shall be ready to use after either the tFEAT time has elapsed or the R/B# signal is back high.

Table 28: Feature Addresses 10h: Programmable Output Drive Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Output drive strength	Not supported						0	0	0	00h	1
	Not supported						0	0	1	01h	
	Not supported						0	1	0	02h	
	50 Ohms						0	1	1	03h	
	37.5 Ohms (default)						1	0	0	04h	
	Not supported						1	0	1	05h	
	Not supported						1	1	X	06h-07h	
Reserved		0	0	0	0	0				00000b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. See Output Drive Impedance for details.

Table 29: Feature Address 30h: V_{PP}

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
External V_{PP} configuration	Disabled (default)								0	0h	
	Enabled								1	1h	1
Reserved		-	-	-	-	-	-	-			
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. This setting controls whether external V_{PP} is enabled. This setting is retained across RESET (FAh, FFh) commands. A HARD RESET (FDh) command will disable the V_{PP} feature and clear the V_{PP} feature address back to its default value for the target LUN.

Table 30: Feature Address 58h: Volume configuration

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Volume Address	Field used to assign a value for a given Volume Address					X	X	X	X		1
Reserved		0	0	0	0					0h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. The host shall only set this feature once per power cycle for each Volume. The address specified is then used in VOLUME SELECT (E1h) command for accessing this NAND Target. This setting is retained across RESET (FAh, FFh) commands. A HARD RESET (FDh) command will not undo any previously set Volume Addressing assignments that were performed prior to the HARD RESET (FDh) command.

Table 31: Feature Addresses 81h: Programmable R/B# Pull-Down Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											

Table 31: Feature Addresses 81h: Programmable R/B# Pull-Down Strength (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
R/B# pull-down strength	Full (default)							0	0	00h	1
	Three-quarter							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

Table 32: Feature Address 83h: Internal/External ZQ Calibration Switching

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Internal/External ZQ Calibration switching	External ZQ calibration (Default)								0	0b	
	Internal ZQ Calibration								1	1b	
Reserved		0	0	0	0	0	0	0		0xh	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

The Internal/External ZQ calibration switching feature allows the user to choose between performing an Internal ZQ calibration or an External ZQ calibration using FA = F8h P1 [0]. By default the part performs an external ZQ calibration, and when FA = F8h P1 [0] = 1, Internal ZQ calibration is performed. The feature is reset when the part is re-initialized via power cycle, or a HARD RESET (FDh) command is issued.

One of the benefits of running Internal ZQ calibration is that it provides a quantifiable upside over without ZQ calibration. External ZQ calibration would still provide the optimal performance upside, but it would require the addition of an external ZQ resistor. Refer to the ZQ calibration section for more details.

Table 33: Feature Address 84h: Clear Extended Status Register

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Reserved		0	0	0	0	0	0	0	0	00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Feature Address 84h: Clear Extended Status Register provides a method for clearing the Extended Status Register (ESR) bits.

Extended Status Register [7:0] bits are persistent until cleared by the host. The host shall issue SET FEATURE BY LUN to Feature Address 84h (Subfeature P1-P4 are don't care) to clear ESR[7:0] to 00h. The host is responsible for clearing the Extended Status Register bits in a timely fashion to ensure that it captures subsequent conditions (Thermal Alert High Limit ESR[1] and Thermal Alert Low Limit ESR[0]). Failure to clear ESR[7:0] quickly may lead to conditions that the firmware may not recognize (example: during cross temperature conditions where both Thermal Alert High and Thermal Alert Low conditions exist on ESR at the same time). GET FEATURE by LUN to Feature Address 84h will return 00h. See Status Operations for more detail on the Extended Status Register.

Table 34: Feature Address 86h: Read Offset Values Reset

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Reserved		0	0	0	0	0	0	0	0	00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Issuing a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to Feature Address 86h will clear all previous stored Read Prefix Offset values stored in Feature Address A0h-ABh to their default values. This is analogous to issuing a HARD RESET (FDh) command or issuing Read Prefix Offset command 2Eh with all offsets set to 00h for each page type (The TLC device would need to have 2Eh command issued 6 times for TLC LP, TLC UP, TLC XP, MLC LP, MLC UP, and SLC).

The Read Prefix Offsets can be reset with Feature Address 86h by setting Subfeatures P1 - P4 to 00h. It will take ^{t}FEAT2 time to fully reset all the read offsets.

Issuing a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to Feature Address 86h is prohibited during cache operations and suspend operations.

Feature Address 86h is non persistent and automatically resets after clearing the offsets. GET FEATURES (EEh) and GET FEATURES by LUN (D4h) commands are prohibited to Feature Address 86h.

To check if all read offsets have been set to 00h on a TLC device, the host can use Feature Address A0h-ABh to read out sub-feature parameters P1 and P2.

Table 35: Feature Address 87h: Sleep Lite

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Sleep Light configuration	Sleep Lite Disable (default)							0	0	00b	
	Sleep Lite Enable							0	1	01b	
	Sleep Lite - Target Level Enable							1	1	11b	
	Reserved	-	-	-	-	-	-				
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

The Sleep Lite feature allows the host to place unselected LUNs on an active target (CE#) into a low power state to reduce overall I_{CC} where the current consumption by any LUN in Sleep Lite will be I_{SB} and I_{SBQ}. This feature only applies to NAND targets where more than one LUN exists per CE#. Once a LUN has been placed in Sleep Lite mode it is unable to accept any host commands.

The Sleep Lite feature will allow for any number of LUNs within a selected target to be placed in a low power state through the use of the SET FEATURES by LUN (D5h) command. When multiple LUNs within a target are to remain active the host will need to issue a SET FEATURES by LUN (D5h) command to each LUN that is to be put into Sleep Lite mode. In the event that the host only wants a single LUN to be active (all other LUNs to be placed into Sleep Lite mode) two different methods exist. The host could issue SET FEATURES by LUN (D5h) commands to each LUN on the target as suggested in the method 1 example. An alternative solution would be for the host to use a target level SET FEATURES (EFh) command with the Sleep Lite - Target Level Enable (P1 = 11b) option as suggested in the method 2 example.

Method 1 for a 2 LUN per CE# configuration example:

1. Issue SET FEATURE by LUN (D5h) command to LUN0 to enable Sleep Lite (P1 = 01b)
2. LUN0 is in Sleep Lite mode. LUN1 remains active.

Method 2 for a 2 LUN per CE# configuration example:

1. LUN1 is selected (could be done using READ STATUS ENHANCED (78h) command or other means)
2. Issue SET FEATURE (EFh) command to enable Sleep Lite - Target Level (P1 = 11b)
3. LUN0 enters Sleep Lite mode. LUN1 remains active.

Because LUNs in Sleep Lite mode cannot accept host commands the only method for exiting Sleep Lite mode is by toggling CE# high for ^{t}CEH. After the CE# signal is pulled HIGH for ^{t}CEH time, CE# is reas-

serted and all LUNs on a target revert to active states. The LUNs exiting Sleep Lite are required to meet the timing parameter specifications for CE# high > 1us even if CE# has not been high for > 1us (e.g. ^{t}CR2 and ^{t}CD).

Since LUNs in Sleep Lite cannot accept commands, if GET FEATURE by LUN (D4h) command is issued to a LUN in Sleep Lite there will be no response. If a GET FEATURE (EEh) command is issued to a Target, the Target response will only be from the LUNs that are not in Sleep Lite and the GET FEATURES (EEh) returned data will specify not in Sleep Lite (P0=00h), hence there is no way to check if any of the LUNs on the Target are in Sleep Lite.

Special consideration is taken in the event that On Die Termination (ODT) is enabled. If the Sleep Lite feature is enabled on a LUN that is configured as a target terminator for the selected volume, that LUN should enter the sniff state. This is the same state the LUN enters if it is configured for non-Target termination and not on the selected volume. If the LUN is configured as a target terminator for the selected volume and a data burst is occurring, ODT should be enabled regardless of the status of the Sleep Lite feature. If a LUN is not configured as a target terminator for the selected volume then it should simply enter Sleep Lite when the Sleep Lite feature is enabled. See On Die Termination (ODT) section for additional details on ODT functionality.

Table 36: LUN state for Matrix Termination with Sleep Lite Feature

LUN is on selected Volume?	Terminator for selected Volume?	Sleep Lite Feature Enabled	LUN State
Yes	No	No	Selected
Yes	No	Yes	Sleep Lite
Yes	Yes	No	Selected
Yes	Yes	Yes	Sniff
No	Yes	N/A	Sniff
No	No	N/A	Deselected

Table 37: Feature Addresses 90h: Array Operation Mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Array Operation Mode	Normal (default)								0	00h	2
	OTP Block								1	01h	1
Reserved		0	0	0	0	0	0	0		0000000b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. See One-Time Programmable (OTP) Operations for details.

2. A RESET (FFh) command will cause the bits of the array operation mode to change to their default values.

Table 38: Feature Address 96h: Auto Read Calibration and Address Cycle Read Retry

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Calibration Read	Calibration disabled with persistence off (default)							0	0	00b	
	Calibration enabled with persistence off							0	1	01b	
	Calibration disabled with persistence on							1	0	10b	
	Calibration enabled with persistence on							1	1	11b	
acrr_enable	ACRR disable (default)						0				
	ACRR enable						1				
Reserved		0	0	0	0	0				00000b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. See Auto Read Calibration and Address Cycle Read Retry section under Read Operations for details and restrictions.

Table 39: Feature Address A0h-ABh Settings

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value
P1										
READ PAGE (00h-30h)/IWL READ (00h-20h) Offset Plane Group X	Read Only	X	X	X	X	X	X	X	X	rSLC, rSLC_edge, r[1-3]_2bpc, r[1-7]_3bpc
P2										
IWL READ (00h-20h) Offset Plane Group Y	Read Only	X	X	X	X	X	X	X	X	rSLC, rSLC_edge, r[1-3]_2bpc, r[1-7]_3bpc
P3										
Calibrated Read Offset Value	Read Only	X	X	X	X	X	X	X	X	rSLC, rSLC_edge, r[1-3]_2bpc, r[1-7]_3bpc
P4										
Reserved		0	0	0	0	0	0	0	0	00h

The read offsets issued via the READ OFFSET PREFIX (2Eh) Command can be read out by the host from FA: A0h-ABh, Subfeature parameter P1 and P2. FA: A0h-ABh are GET only registers.

See FEATURE ADDRESS A0h-ABh Settings Section of the Datasheet for more information on Feature Address assignments and offset readout resolution.

Table 40: Feature Addresses B1h-B4h, E1h-E3h: SBSBR

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
offset level	See Note 2	X	X	X	X	X	X	X	X	XXh	1
P2											
offset level	See Note 2	X	X	X	X	X	X	X	X	XXh	1
P3											
offset level	See Note 2	X	X	X	X	X	X	X	X	XXh	1
P4											
offset level	See Note 2	X	X	X	X	X	X	X	X	XXh	1

Notes: 1. See the Definitions for Feature Addresses B1h-B4h, E1h-E3h table in the SBSBR Operations sub-section, for read level references
2. See the P1, P2, P3, P4 Subfeature Values and Corresponding Offset Voltage for Feature Addresses B1h-B4h, E1h-E3h table in the SBSBR Operations sub-section, to determine the subfeature value for a desired offset voltage

Table 41: Feature Address DAh: Thermal Alert

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Thermal Alert Feature	Disable(Default)								0	00h	
	Enable								1	01h	
Reserved		0	0	0	0	0	0	0		0000000b	
P2											
temp_l (User Input)	-37C Example Input (Default)	0	0	0	0	0	0	0	0	00h	1
	-36C Example Input	0	0	0	0	0	0	0	1	01h	
	-	X	X	X	X	X	X	X	X		
	124C Example Input	1	0	1	0	0	0	0	1	A1h	
	125C Example Input	1	0	1	0	0	0	1	0	A2h	
P3											
temp_h (User Input)	-37C Example Input (Default)	0	0	0	0	0	0	0	0	00h	1
	-36C Example Input	0	0	0	0	0	0	0	1	01h	
	-	X	X	X	X	X	X	X	X		
	124C Example Input	1	0	1	0	0	0	0	1	A1h	
	125C Example Input	1	0	1	0	0	0	1	0	A2h	
P4											

Table 41: Feature Address DAh: Thermal Alert (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. The values in P2[7:0] temp_l and P3[7:0] temp_h are ignored by the LUN until FA DAh P1[0] is set to a 1 and a thermal evaluation event occurs. Thermal evaluation only occurs during valid program/read/erase operations.

The Thermal Alert Feature provides the host with information regarding the NAND's internal operating temperature by updating the status register values after every valid array operation. With this feature, the host is allowed to configure the lower (temp_l) and upper (temp_h) temperature boundaries, and when the NAND operates outside the user specified temperature range the host is alerted of this change. This feature reduces the hosts need to poll for the NAND temperature and offers a quick way to monitor the NAND's temperature.

To enable Thermal Alert feature, user needs to set FA DAh [P1_0] to 1, the feature is disabled by default. It is the responsibility of the user to configure temp_l (FA DAh [P2_7:0])and temp_h (FA DAh [P3_7:0]) within valid range -37°C to +125°C. When Thermal Alert feature is enabled, NAND evaluates the temperature against thresholds (i.e. temp_h and temp_l).

To disable Thermal Alert feature, user must set the FA DAh [P1:0] to 0. With the feature disabled, temp_l and temp_h are ignored, even if their values were in the valid temperature range, and there would be no set to the Status Register bit SR[4] value due to thermal alert, and no new set of Extended Status Register bit Thermal Alert High Limit ESR[1], and no new set of Extended Status Resister bit Thermal Alert Low ESR[0].

Thermal evaluation occurs only during valid program/read/erase operations. Based on thermal condition, the NAND sets Status Register flag bit SR[4], Extended Status Register bit Thermal Alert High Limit ESR[1], and Extended Status Resister bit Thermal Alert Low ESR[0] to one or zero. SR[4], ESR[1], and ESR[0] are updated together during the algo when RDY (SR[6]) = 1 and ARDY (SR[5]) = 1 or 0. Thermal Alert is evaluated for bad blocks but SR[4], ESR[1], and ESR[0] are considered invalid. For Program and Erase operations, if the operation is invalidated by Lock status (SR[7] = 0) then no Thermal Alert is evaluated. Status Register bit SR[4] is used for Thermal Alert High Limit and Thermal Alert Low Limit. Extended Status Register bits are read out by command status 79h. Extended Status Register bit Thermal Alert High Limit ESR[1] and Extended Status Resister bit Thermal Alert Low ESR[0] bits are persistent until cleared by the host. See Status Operations section for more information on Status Register and Extended Status Register operation.

The thermal alert feature will support temperature range similar to the temperature readout through GET FEATURE (EEh). The feature has a range of -37°C to +125°C. The temperature readout is targeted to an accuracy of ±5°C between the temperatures of 70°C to 0°C. Accuracies are sampled and not 100% tested.

In addition, host can enable Thermal Level detection by independently configuring temp_l and temp_h. For example, setting temp_l=00h and configuring temp_h to the desired value can help detect if NAND goes above temp_h. Similarly, setting temp_h=FFh and configuring temp_l to desired value can help detect if NAND goes below temp_l value.

Condition when Extended Status Register bit Thermal Alert High Limit ESR[1] is set to 0 and when Extended Status Register bit Thermal Alert Low Limit ESR[0] is set to 0:

- NAND temp_l <= NAND temp <= temp_h

Condition when Extended Status Register bit Thermal Alert High Limit ESR[1] is set to 1 and when Extended Status Register bit Thermal Alert Low Limit ESR[0] is set to 0:

- NAND temp > temp_h

Condition when Extended Status Register bit Thermal Alert High Limit ESR[1] is set to 0 and when Extended Status Register bit Thermal Alert Low Limit ESR[0] is set to 1:

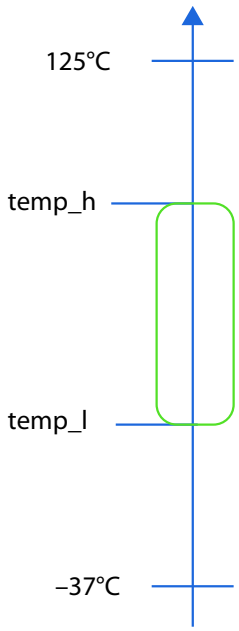
- NAND temp < temp_l

Condition when Extended Status Register bit Thermal Alert High Limit ESR[1] is set to 1 and when Extended Status Register bit Thermal Alert Low Limit ESR[0] is set to 1:

- NAND temp < temp_l and NAND temp > temp_h (can occur if Host does not clear ESR[7:0] in a timely fashion)

The user shall not set temp_l value higher than the temp_h value. Temp_l can only be set less than or equal to temp_h.

Figure 56: Thermal Status Alert Illustration



Thermal alert status is valid when RDY (SR[6]) = 1 and ARDY (SR[5]) = 1 or 0. Thermal alert status at RDY (SR[6]) = 1 reflects thermal alert status of current valid NAND array operations.

Table 42: NAND Operations and Thermal Alert

NAND Array Operation	Extended Status Register bit Thermal Alert High Limit ESR[1] valid and/or Extended Status Register bit Thermal Alert Low Limit ESR[0] valid
READ PAGE (00h-30h)	Yes
READ PAGE CACHE SEQUENTIAL (31h)	Yes
READ PAGE CACHE RANDOM (00h-31h)	Yes
READ PAGE CACHE LAST (3Fh)	Yes
IWL READ (00h-20h)	Yes
READ UNIQUE ID (EDh)	Yes
READ PARAMETER PAGE (ECh)	Yes
Single Bit page Soft Read (00h-34h)	Yes
Reads that invoke Feature Address 96h: Auto Read Calibration functionality	Yes

Table 42: NAND Operations and Thermal Alert (Continued)

NAND Array Operation	Extended Status Register bit Thermal Alert High Limit ESR[1] valid and/or Extended Status Register bit Thermal Alert Low Limit ESR[0] valid
Reads that invoke Feature Addresses A0h-ABh functionality	Yes
GET FEATURE (EEh) / SET FEATURE (EFh)	No [1]
PROGRAM PAGE (80h-10h)	Yes
PROGRAM PAGE CACHE (80h-15h)	Yes
PROGRAM SUSPEND (84h)	Yes
PROGRAM RESUME (13h)	Yes
ERASE BLOCK (60h-D0h)	Yes
ERASE SUSPEND (61h)	Yes
ERASE RESUME (D2h)	Yes
All RESETs	No [1]

Notes: 1. RESET and GET FEATURE/SET FEATURE operations will clear the thermal alert status bit in SR[4] to 0. SR[4], ESR[1], and ESR[0] bits will be invalid for Thermal Alert before RDY (SR[6]) goes high. Extended Status Register bit Thermal Alert High Limit ESR[1] and Extended Status Resister bit Thermal Alert Low ESR[0] are cleared by SET FEATURE BY LUN to Feature Address 84h)

Table 43: Feature Address E7h: Temperature Sensor Readout

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Temperature Sensor Readout	-37°C example output	0	0	0	0	0	0	0	0	00h	1, 2
	-36°C example output	0	0	0	0	0	0	0	1	01h	
	-	X	X	X	X	X	X	X	X		
	89°C example output	0	1	1	1	1	1	1	0	7Eh	
	90°C example output	0	1	1	1	1	1	1	1	7Fh	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. Each bit is 1°C. For example, an output of 55h is roughly 48°C. The temperature readout is targeted to an accuracy of ±5°C between the temperatures of 70°C to 0°C. Accuracies are sampled and not 100% tested.
2. Device reading out temperature beyond specified operational temperature ranges for a given device does not meant to signify support of those temperatures.

Only a GET FEATURES (EEh) or GET FEATURES by LUN (D4h) commands are permitted to feature address E7h, SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands are not supported to feature address E7h. The temperature sensor shall return the current temperature value no more than ^{t}TEMP after the host controller issues the GET FEATURES (EEh) or GET FEATURES by LUN (D4h) command to feature address E7h. GET FEATURES (EEh) and GET FEATURES by LUN (D4h) commands are not supported to feature address E7h when the target (CE#) or target LUN is in any busy state.

If there is only 1 LUN per CE# of a NAND device, then either the GET FEATURES (EEh) or GET FEATURES by LUN (D4h) command can be used to access the Temperature Sensor Readout (Feature Address E7h). If there is more than one LUN per CE#, then the GET FEATURES by LUN (D4h) command shall be used to access the Temperature Sensor Readout (Feature Address E7h), not the GET FEATURES (EEh) command, to avoid possible data contention.

Table 44: Temperature Sensor Readout Parameter

Parameter	Symbol	Min	Max	Units
Busy time for GET FEATURES operation for Temperature Sensor readout	^{t}TEMP	–	35	µs

VOLUME SELECT (E1h)

The VOLUME SELECT function is used to select a particular volume based on the address specified. VOLUME SELECT (E1h) command is required to be used when matrix termination is used.

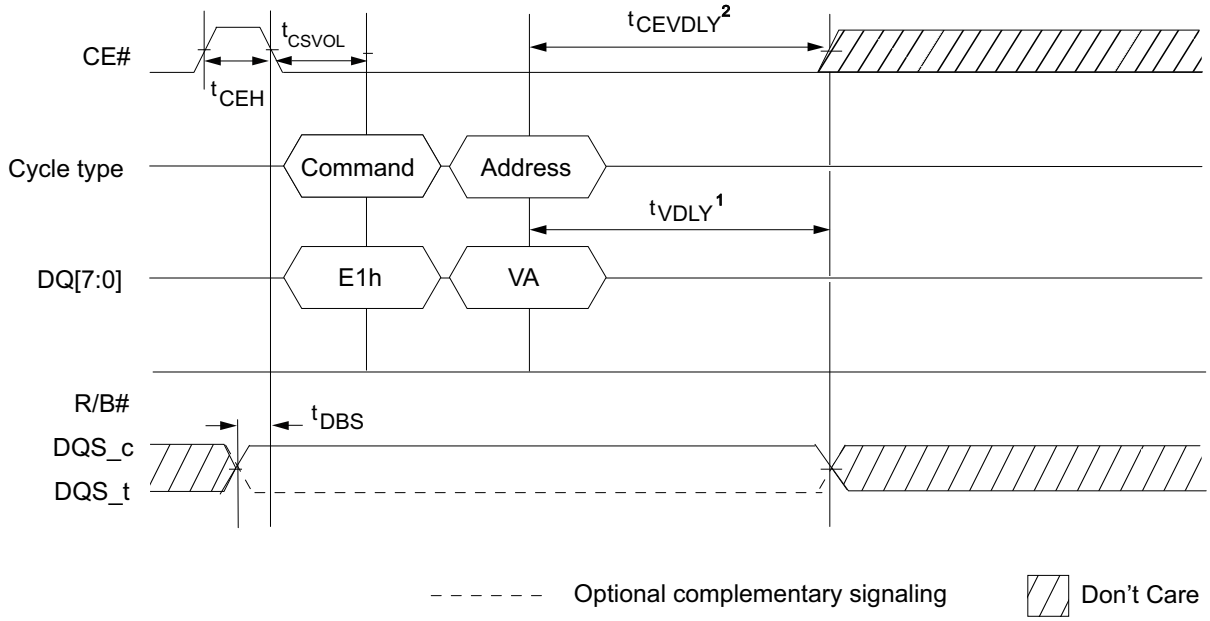
This command is accepted by all targets that share a particular CE# pin. The command may be executed with any LUN on the volume in any state. The VOLUME SELECT (E1h) command may only be issued as the first command after CE# is pulled LOW; CE# shall have remained HIGH for ^{t}CEH and CE# LOW for at least ^{t}CSVOL prior to the command in order for the VOLUME SELECT (E1h) command to be properly received by all NAND targets connected to the host target. The DQS (DQS_t) signal shall remain HIGH for the entire VOLUME SELECT command sequence.

When the VOLUME SELECT (E1h) command is issued, all NAND targets that have a volume address that does not match the address specified shall be deselected to save power (equivalent behavior to CE# pulled HGH). If one of the LUNs in an unselected volume is the assigned terminator for the volume addressed, then that LUN will enter the sniff state.

If the volume address specified does not correspond to any appointed volume address, then all NAND targets shall be deselected until a subsequent VOLUME SELECT (E1h) command is issued. If the VOLUME SELECT (E1h) command is not the first command issued after CE# is pulled LOW, then the NAND targets revert to their previous selected, deselected, or sniff states.

The volume address is retained across RESET (FAh, FFh) commands. A HARD RESET (FDh) command will not undo any previously set volume addressing assignments that were performed prior to the HARD RESET (FDh) command. After HARD RESET (FDh) command is issued the NAND targets do not revert to their previous selected, deselected, or sniff states and a VOLUME SELECT command (E1h) is required to select the desired volume.

Figure 57: VOLUME SELECT (E1h) Operation



Notes: 1. The host shall not issue new commands to any LUN on any volume until after ^{t}VDLY. This delay is required to ensure the appropriate volume is selected for the next command issued. See Multiple Volume Operations Restrictions section for restrictions and requirements related to operations across multiple volumes.

2. The host shall not bring CE# HIGH on any volume until after ^{t}CEVDLY. This delay is required to ensure the appropriate volume is selected based on the previously issued VOLUME SELECT command.

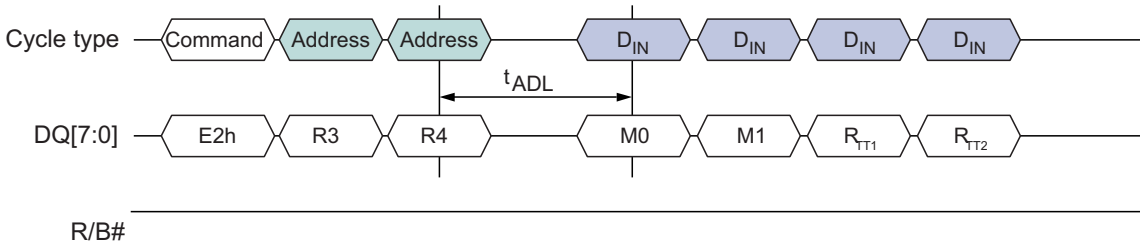
Table 45: Volume Address

Description	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Volume Address											
VA						Volume address				–	
Reserved		0	0	0	0					–	

ODT CONFIGURE (E2h)

The ODT CONFIGURE (E2h) command is used to configure on-die termination. Specifically, ODT CONFIGURE (E2h) specifies whether a particular LUN is a terminator for a volume(s) and the R_{TT} settings. If the LUN is specified as a terminator for one or more volumes, then the LUN shall enable on-die termination when either data input or data output cycles are executed on the volume(s) it is acting as a terminator for depending on the settings of ODT Configuration Matrix Table . The on-die termination settings are retained across RESET (FAh, FFh) commands, but are not retained across HARD RESET (FDh) commands for the target LUN.

Figure 58: ODT CONFIGURE (E2h) Operation



The LUN address correspond to the same structure as the address cycles for the NAND device which determine which LUN will act as the terminator.

The ODT configuration matrix structure is defined in table below. For the volume address fields M0 and M1, if a bit is set to one then the LUN shall act as the terminator for the corresponding volume(s) (Vn) where n corresponds to the volume address.

If host issues ODT CONFIGURE (E2h) command during a program data load sequence, first the data load sequence must be closed and internal pipeline flushed with an 11h command prior to issuing the command.

Table 46: ODT Configuration Matrix

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value
M0 – Lower byte of the ODT configuration matrix										
Volume address	Volumes that will be terminated by selected LUN	V7	V6	V5	V4	V3	V2	V1	V0	–
M1 – Upper byte of the ODT configuration matrix										
Volume address	Volumes that will be terminated by selected LUN	V15	V14	V13	V12	V11	V10	V9	V8	–
R_{TT1}										
DQ[7:0]/DQS_t/DQS_c R_{TT} and ODT enable for data input	ODT disabled (default)					0	0	0	0	0h
	ODT enabled with R_{TT} of 150 ohms					0	0	0	1	1h
	ODT enabled with R_{TT} of 75 ohms					0	0	1	1	3h
	ODT enabled with R_{TT} of 50 ohms					0	1	0	0	4h
Reserved	–					0	0	1	0	2h
						0	1	0	1	5h
						0	1	1	0	6h
						0	1	1	1	7h
						1	X	X	X	8h–Fh

Table 46: ODT Configuration Matrix (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value
DQ[7:0]/DQS_t/DQS_c R_{TT} and ODT enable for data output	ODT disabled (default)	0	0	0	0					0h
	ODT enabled with R_{TT} of 150 ohms	0	0	0	1					1h
	ODT enabled with R_{TT} of 75 ohms	0	0	1	1					3h
	ODT enabled with R_{TT} of 50 ohms	0	1	0	0					4h
Reserved	–	0	0	1	0					2h
		0	1	0	1					5h
		0	1	1	0					6h
		0	1	1	1					7h
		1	X	X	X					8h–Fh
R_{TT2}										
RE_t and RE_c R_{TT} ODT enable	ODT disabled (default)					0	0	0	0	0h
	ODT enabled with R_{TT} of 150 ohms					0	0	0	1	1h
	ODT enabled with R_{TT} of 75 ohms					0	0	1	1	3h
	ODT enabled with R_{TT} of 50 ohms					0	1	0	0	4h
Reserved	–					0	0	1	0	2h
						0	1	0	1	5h
						0	1	1	0	6h
						0	1	1	1	7h
						1	X	X	X	8h–Fh
Reserved	–	0	0	0	0					0h

ODT CONFIGURE (E2h) for LUNs Operating in Mirrored Mode

When issuing the ODT CONFIGURE (E2h) command sequence to a LUN operating in electronic mirroring mode, the host must issue the mirrored version of M0, M1, R_{TT1}, R_{TT2} data. As an example, the table below shows the required data for M0, M1, R_{TT1}, and R_{TT2} for LUNs in Non-mirror Mode and Mirror Mode. As shown in the table below, in order to configure a Mirror Mode LUN for Vol0 ODT operations, then the host must issue an 80h on M0 instead of 01h, where the mirrored version of 01h (0000 0001b) is 80h (1000 0000b). Likewise, in order to configure a Mirror Mode LUN to 150 Ohms ODT for data output and 75 Ohms ODT for data input, the host must issue a C8h for R_{TT1} instead of 13h, since the mirrored version of 13h (0001 0011b) is C8h (1100 1000b). Finally, in order to configure a Mirror Mode LUN to 50 Ohms ODT on RE_t/RE_c during data output, then the host must issue a 20h for RTT2 instead of 04h, where the mirrored version of 04h (0000 0100b) is 20h (0010 0000b).

Table 47: Example of ODT Matrix Configuration for LUNs in Non-Mirrored and Mirrored Modes

Bus Cycle	Bus Cycle Description	Non-Mirror Mode LUNs		Mirror Mode LUNs	
		Required DQ[7:0] at Controller	Required DQ[7:0] at Package Balls	Required DQ[7:0] at Controller	Required DQ[7:0] at Package Balls
E2h Command	E2h Command	E2h	E2h	E2h	47h
R3 Address	LUN Address R3=00h, R4=01h	00h	00h	00h	00h
R4 Address		01h	01h	01h	80h
M0	Enable ODT Operations on LUN for Vol0 only	01h	01h	80h	01h
M1		00h	00h	00h	00h
R_{TT1}	Enable 150 Ohms ODTfor data output and 75 Ohms ODT for data input on DQ[7:0], DQS_t/DQS_c	13h	13h	C8h	13h
R_{TT2}	Enable 50 Ohms ODTfor RE_t/RE_c for data output	04h	04h	20h	04h

ZQ Calibration

ZQ Calibration is performed by issuing F9h command for ZQCL (ZQ long calibration) and D9h command for ZQCS (ZQ short calibration). ZQ Calibration is used to calibrate NAND R_{ON} values. A longer time is required to calibrate output driver circuits at initialization and relatively smaller time to perform periodic calibrations.

The ZQCL (F9h) command is used to perform the initial calibration after power-up initialization sequence. The command enable ZQCL (F9h) may be issued at any time by the controller depending on the system environment. ZQCL (F9h) triggers the calibration engine inside the NAND device and once calibration is achieved, the calibrated values are transferred from the calibration engine to NAND I/O signals, which gets reflected as updated output driver values

ZQCL (F9h) operations are allowed a timing period of ^{t}ZQCL to perform the full calibration and then transfer of output driver values. When ZQCL (F9h) operation is complete, the host shall check status. If the FAIL bit is set (that is, SR[0] = 1), then the calibration procedure failed and user should check the RZQ resistor connection. If ZQCL (F9h) calibration fails the device will use the optimal driver settings.

ZQCS (D9h) command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter ^{t}ZQCS. One ZQCS (D9h) command can effectively correct a minimum of 1.5% (ZQ Correction) of R_{ON} impedance error within ^{t}ZQCS for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' table. The appropriate interval between ZQCS (D9h) commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS (D9h) commands, given the temperature ($T_{Driftrate}$) and voltage ($V_{Driftrate}$) drift rates that the NAND is subject to in the application, is illustrated below. The interval could be defined by the following formula:

Figure 59: Calibration Time Interval Equation

$$Interval = \frac{ZQCorrection}{[(T_{SENS} \times T_{Driftrate}) + (V_{SENS} \times V_{Driftrate})]}$$

Where T_{SENS} = max($dR_{TT}dT$, $dR_{ON}dTM$) and V_{Sens} = max ($dR_{TT}dV$, $dR_{ON}dVM$) define the NAND temperature and voltage sensitivities. For example, if T_{Sens} = 0.5%/°C, V_{Sens} = 0.2%/mV, $T_{Driftrate}$ = 1°C/sec and $V_{Driftrate}$ = 15 mV/sec, then the interval between ZQCS (D9h) commands is calculated as:

Figure 60: Example of Interval Calculation between ZQCS (D9h) Commands

$$\frac{1.5}{[(0.5 \times 1) + (0.2 \times 15)]} = 0.429 = 429ms$$

No other activities, including STATUS (70h/78h) operations, should be performed on the NAND channel (that is, data bus) by the controller for the duration of ^{t}ZQCL or ^{t}ZQCS. The quiet time on the NAND channel allows accurate calibration of output driver and on-die termination values. For multi-channel packages, all channels should not have any data transfer occur during ZQ calibration even if not a shared channel with the LUN performing ZQ calibration. Once NAND calibration is achieved, the NAND should disable ZQ current consumption path to reduce power. NAND array operations may not occur on the device performing ZQCL (F9h) or ZQCS (D9h) operations. NAND array operations may occur on any devices that share the ZQ resistor with the device performing ZQCL (F9h) or ZQCS (D9h) operations. All devices connected to the DQ bus shall be in high impedance during the calibration procedure. The R/B# signal will be brought LOW by the device during calibration time, but if other deviecs are driving a shared R/B# LOW then the host is required to wait the maximum ^{t}WB + ^{t}ZQCL or ^{t}ZQCS time before issuing any commands to the data bus.

If a RESET (FFh, FAh) command is issued during a ZQ calibration operation, the calibration operation is interrupted and the RESET (FFh, FAh) operation is executed. After the RESET (FFh, FAh) command, the host is required to issue a new calibration command as soon as possible. The host is required to issue the ZQCL (F9h) command if the RESET (FFh, FAh) command is issued during ZQCL. If the RESET (FFh, FAh) command was issued during the ZQCL (F9h) operation, the NAND device will revert to factory settings for output driver strength values (that is, as if no ZQ calibration operation was performed). If the RESET (FFh, FAh) command was issued during ZQCS (D9h) operation the NAND device will use the calibrated values from the last successful calibration operation. The host is required to issue a ZQCS (D9h) command as soon as possible and to let the ZQCS operation run to completion without interruption prior to issuing a ZQCL (F9h) command.

ZQ Calibration Long (F9h)

The ZQ CALIBRATION LONG (ZQCL) (F9h) command is used to perform the initial calibration. Writing F9h to the command register, followed by one row address cycle containing the LUN address, begins the ZQCL (F9h) on the selected LUN. This command may be issued at any time by the host, depending on the system environment. The ZQCL (F9h) command triggers the calibration engine inside the NAND. After calibration is achieved, the calibrated values are transferred from the calibration engine to the NAND I/Os, which are reflected as updated R_{ON} values.

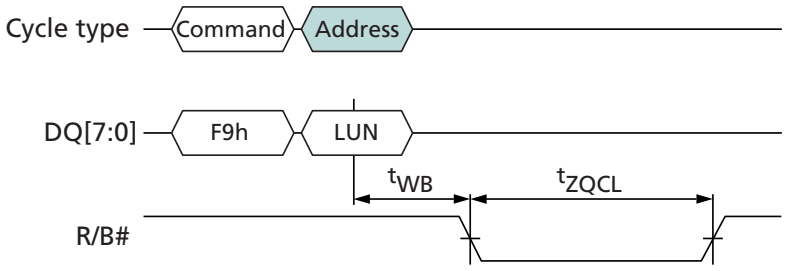
During ZQCL (F9h) operations, no array operations are allowed on the NAND device that is performing the ZQCL (F9h) operation. Array operations are allowed on any of the other NAND devices that share the ZQ signal with the NAND device that is performing the ZQCL (F9h) operation.

The NAND is allowed a timing window defined by either ^{t}ZQCL to perform a full calibration and transfer of values. When ZQCL (F9h) is issued during the initialization sequence, the timing parameter ^{t}ZQCL must be satisfied.

If a RESET (FFh, FAh) command is issued during ZQCL, the calibration operation is interrupted and the RESET (FFh, FAh) operation is executed. The NAND device will revert to factory settings for output driver strength values (that is, as if no ZQ calibration operation was performed). The host is required to issue ZQCL (F9h) command as soon as possible.

When ZQCL (F9h) operation is complete, the host shall check status. If the FAIL bit is set (that is, SR[0] = 1), then the calibration procedure failed and user should check the R_{ZQ} resistor connection. If the ZQCL (F9h) operation fails the device will use the optimal driver settings.

Figure 61: ZQ Calibration Long (F9h)



ZQ Calibration Short (D9h)

The ZQ CALIBRATION SHORT (ZQCS) command (D9h) is used to perform periodic calibrations to account for small voltage and temperature variations. Writing D9h to the command register, followed by one row address cycle containing the LUN address, begins the ZQCS (D9h) on the selected LUN. A shorter timing window is provided to perform the reduced calibration and transfer of values as defined

by timing parameter ^{t}ZQCS. A ZQCS (D9h) command can effectively correct a minimum of 1.5% R_{ON} impedance error within ^{t}ZQCS, assuming the maximum sensitivities specified in the Output Driver Voltage and Temperature Sensitivity table.

During a ZQCS (D9h) operation, no array operations are allowed on the NAND device that is performing the ZQCS (D9h) operation. Array operations are allowed on any of the other NAND devices that share the ZQ signal with the NAND device that is performing the ZQCS (D9h) operation.

When the ZQCS (D9h) operation is complete, the host shall check status. If the FAIL bit is set (that is, SR[0] = 1), then the calibration procedure failed and user should issue ZQCL (F9h) command. If the ZQCS (F9h) operation fails the device will use the optimal driver settings, but output driver strength may still not be within specified range. If after the ZQCS (D9h) operation fails and subsequent ZQCL (F9h) operation passes, the NAND device output driver strength is within specified range and the calibration sequence was successful. The user should not rerun the ZQCS (D9h) operation in this case. If after the ZQCS (D9h) operation fails and subsequent ZQCL (F9h) operation fails, the NAND device output driver strength is not within specified range and the calibration sequence was unsuccessful. In this case, the device has the optimal driver settings, but signal integrity issues may occur.

When a RESET (FFh, FAh) command is issued during ZQCS, the calibration operation is interrupted and the RESET (FFh, FAh) operation is executed. The NAND device will use the calibrated values from the last successful calibration operation. The host is required to issue a ZQCS (D9h) command as soon as possible and to let the ZQCS operation run to completion without interruption prior to issuing a ZQCL (F9h) command.

Figure 62: ZQ Calibration Short (D9h)

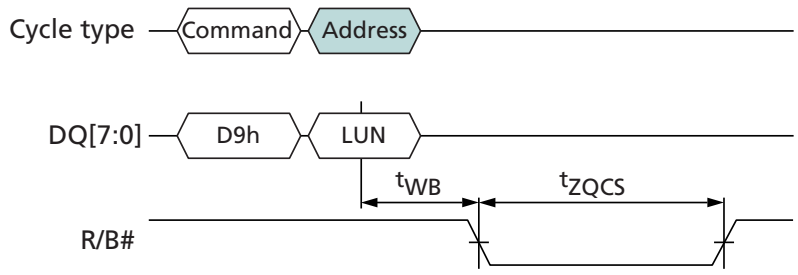


Table 48: LUN Address Cycle Decoding

Description	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
LUN											
Bits LA0 (DQ0) and LA1 (DQ1) for LUN selection	LUN0							0	0	–	
	LUN1							0	1	–	
	LUN2							1	0	–	
	LUN3							1	1	–	
Reserved	Don't Care	–	–	–	–	–	–			–	1

Notes: 1. Can be either 1 or 0.

ZQ External Resistor Value, Tolerance, And Capacitive Loading

In order to use the ZQ Calibration function, a 300 ohm ±1% tolerance external resistor must be connected between the ZQ pin and ground. The ZQ resistance is the sum of the trace resistance and the actual resistor resistance. The user should attempt to place ZQ resistor as close as possible to the

NAND device to reduce the trace resistance. The resistance presented to the NAND needs to be ±1% of 300 ohms. The single resistor can be used for each NAND or one resistor can be shared between all NAND devices in the package if the ZQ calibration timings for each NAND do not overlap. The capacitance of the LUN component of the ZQ signal will be less than an I/O signal. Depending on the number of LUNs per package, the total capacitance (capacitance of package + capacitance of LUN(s)) of the ZQ signal may exceed an I/O signal. For packages with eight or more LUN that share a ZQ signal, the total ZQ capacitance will not exceed 15% greater than the number of LUNs times the LUN capacitance of an I/O signal [that is, Total ZQ capacitance < 1.15 * LUN capacitance (I/O) * number of LUNs].

The NV-DDR3 driver supports two different R_{ON} values. These R_{ON} values are R_{ON} = 37.5 ohms and 50 ohms. Output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ} as follows:

- $R_{ON}37.5 = R_{ZQ}/8$ (nominal 37.5 ohms ±15% with nominal R_{ZQ} = 300 ohms)

Table 49: I/O Drive Strength Settings

Interface	Setting	Drive Strength	V_{CCQ}	Notes
NV-DDR3	37.5 ohms	RZQ/8	1.2V	
	50 ohms	RZQ/6		

Status Operations

Each die (LUN) provides its status independently of other die (LUNs) on the same target through its 8-bit Status Register SR[7:0] and its 8-bit Extended Status Register ESR[7:0].

The 8-bit Status Register will provide status of the device for WP# SR[7], RDY SR[6], ARDY SR[5], ESR flag bit SR[4], Program Suspend SR[3], Erase Suspend SR[2], FailC SR[1], and Fail SR[0]. The 8-bit Extended Status Register will provide status of the device for Thermal Alert High Limit ESR[1] and Thermal Alert Low Limit ESR[0]. Status Register Flag bit SR[4] in the 8-bit Status Register and the Extended Status Register ESR[1:0] bits will be updated together during an algo (array and non-array) and is valid when RDY (SR[6]) = 1 and ARDY (SR[5]) = 1 or 0.

Program Suspend SR[3] is persistent and will always reflect if a program is suspended on the LUN. Erase Suspend SR[2] is persistent and will always reflect if an erase is suspended on the LUN. Program Suspend SR[3] = 1 is valid after a Program Suspend [84h] command and ADRY transitions from zero to one until the suspended program is resumed or RESET (FFh, FAh, FDh) is issued. The Erase Suspend SR[2] = 1 is valid after an Erase Suspend [61h] command and ARDY transitions from zero to one until the suspended erase is resumed or RESET (FFh, FAh, FDh) is issued. The persistence of program and erase suspend provides the host with a method for monitoring a suspend status without tying up system resources or missing a suspend event. Please see Program Suspend and Erase Suspend sections for more detail.

SR[4] is the Status Register Flag Bit. Power-on default is SR[4] = 1. Status Register Flag Bit SR[4] value is updated by Thermal Alert during an algo (array or non-array) and is valid when RDY (SR[6]) = 1 and ARDY (SR[5]) = 1 or 0. The Status Register flag bit SR[4] can be detected by the host with READ STATUS (70h), READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command. The host can monitor the 8-bit Status Register for Status Register flag bit SR[4] = 1 and when detected, it must issue the EXTENDED STATUS REGISTER READ (79h) for the 8-bit Extended Status Register ESR[7:0] to determine the cause of the Status Register flag bit = 1. Status Register flag bit SR[4] and EXTENDED STATUS REGISTER READ (79h) are valid when RDY (SR[6]) = 1 and ARDY (SR[5]) = 1 or 0. Any READ STATUS command (70h/78h/71h) should be issued before the next command so as not to lose Status Register Flag Bit SR[4] bit information since it gets reset every time RDY(SR[6]) goes LOW.

The Status Register flag bit SR[4] also keeps track of any Thermal Alert events during a Program, Erase, or Nested suspend/resume operations. The NAND will always check for any possible ESR Flag bit events for the duration of the operation and store SR[4] status accordingly. Upon completion of the operation, the final SR[4] status and ESR flag bits should reflect any event that occurred regardless of whether it happened at the start, suspend, or resume states. This NAND behavior provides the host with critical information that may require some error handling after an operation has completed.

When any single event or combination of Thermal Alert (high/low)/and RESET (FFh, FAh, FDh) command, before RDY (SR[6]) goes high, the Status Register flag bit (SR[4]) and Status Register 79h will be INVALID.

Extended Status Register [7:0] bits are persistent until cleared by the host. The host shall issue SET FEATURE BY LUN to Feature Address 84h (Subfeature P1-P4 are don't care) to clear ESR[7:0]. The host is responsible for clearing the Extended Status Register bits in a timely fashion to ensure that it captures subsequent conditions that can occur to set Thermal Alert High Limit ESR[1] or Thermal Alert Low Limit ESR[0] = 1. Error events for Thermal Alert will accumulate between the SET FEATURE by LUN to Feature Address 84h commands.

After the READ STATUS (70h), READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command is issued, status register output is enabled. The contents of the status register are returned on DQ[7:0] for each data output request.

After the EXTENDED STATUS REGISTER READ (79h) command is issued, Extended Status Register output is enabled. The contents of the Extended Status Register are returned on DQ[7:0] for each data output request.

When LUN is active and Status Register output is enabled, changes in the Status Register are seen on DQ[7:0] as long as CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

The READ STATUS (70h) command returns the status of the most recently selected die (LUN). To prevent data contention during or following an interleaved die (multi-LUN) operation, the host must enable only one die (LUN) for status output by using the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command, or for extended status register output by using the EXTENDED STATUS REGISTER READ (79h) command; (see Interleaved Die (Multi-LUN) Operations).

IWL/Cache Operations: During IWL Read (Independent Word Line Read) operations and Cache operations, since Status Register flag bit SR[4] is cleared at the start of any new algo, an SR[4] event may be missed.

- IWL operations: Status Register flag bit SR[4] is shared between plane groups and may miss events
- Cache Operations: Thermal Alert is set when RDY (SR[6]) = 1 and ARDY (SR[5]) = 1 or 0 and is valid until a new operation starts

ESR[7:0] will be updated in all IWL Read and Cache operation when RDY (SR[6]) = 1 and ARDY (SR[5]) = 1 or 0 and will be persistent and provide the host ability to always catch missed Status Register flag bit SR[4] events.

Each die (LUN) provides unique SR[6] and SR[5] register bits by plane group for IWL Read Operations. RDY (RB#) for the die (LUN) is an AND of the SR[6] values of all plane groups. For the host to determine a unique SR[6] plane group value during IWL Read Operations, the use of the READ STATUS ENHANCED (78h) to address the required plane group's status register SR[6] bit will be necessary. The READ STATUS (70h) and FIXED ADDRESS READ STATUS ENHANCED (71h) will result in a RDY (RB#) busy if either of the plane groups are busy. For the host to determine a unique ARDY SR[5] plane group value during IWL Read Operations, the use of the READ STATUS ENHANCED (78h) to address the required plane group's status register SR[5] bit will be necessary. The READ STATUS (70h) and FIXED ADDRESS READ STATUS ENHANCED (71h) will result in a SR[5] busy if either of the plane groups are busy.

Table 50: Status Register (SR) Definition

SR Bit	Definition	Independent per Plane Group[1]	Description
7	WP#[2]	–	Write Protect: 0 = Protected 1 = Not protected In the normal array mode, this bit indicates the value of the WP# signal. In OTP mode this bit is set to 0 if a PROGRAM OTP PAGE operation is attempted and the OTP area is protected. This bit is valid only when ARDY (SR bit 5) is 1.
6	RDY[3]	Yes	Ready/Busy I/O: 0 = Busy 1 = Ready This bit indicates that the selected die (LUN) is not available to accept new commands, address, or data I/O cycles with the exception of RESET LUN (FAh), RESET (FFh), READ STATUS (70h), and READ STATUS ENHANCED (78h). This bit applies only to the selected die (LUN).
5	ARDY[3]	Yes	Ready/Busy Array: 0 = Busy 1 = Ready This bit goes LOW (busy) when an array operation is occurring on any plane of the selected die (LUN). It goes HIGH when all array operations on the selected die (LUN) finish. This bit applies only to the selected die (LUN).
4	ESR Flag Bit: V_{CC} Alert/Thermal Alert High or Low[4]	–	ESR Flag Bit: 0 = default 1 = Error event from ESR[7:0] or Power-on default. The NAND will set the SR bit 4, when V_{CC} min is violated during an ongoing Read, Program, or Erase operation (e.g. SR[5] = 0), or a Thermal Alert Status Temperature is outside (low or high) the defined temperature range after valid NAND array operation. This bit is valid only when RDY (SR[6]) = 1 and ARDY (SR[5]) = 1 or 0. Power-on default for SR bit 4 = 1. During array operations, SR[4]=1 can indicate Vcc min violation, but SR[4]=0 does not indicate the absence of Vcc min violation
3	PROGRAM SUSPEND	–	Program Suspend: Used in conjunction with FAILC/FAIL of the status register (SR[1]/SR[0]) SUSPEND is persistent and will remain set until the Program Suspend operation is finished after Program Resume or a RESET (FFh, FAh, FDh) is issued. SUSPEND = 0, FAIL = 0: Program operation completed with successful status. SUSPEND = 0, FAIL = 1: Program operation completed with fail status. SUSPEND = 1, FAIL = 0: Program operation successful suspended SUSPEND = 1, FAIL = 1: This state will not exist. Fail will always be "0" in Suspend State FAILC is valid only in the initial Suspend State (SUSPEND=1) and provides fail status for previous program immediately completed prior to suspended program operation FAILC is invalid for any operations performed after suspend is issued and for the Resumed array operation from Suspend State. This bit is valid only when ARDY (SR[5]) or RDY (SR[6]) is 1.

Table 50: Status Register (SR) Definition (Continued)

SR Bit	Definition	Independent per Plane Group[1]	Description
2	ERASE SUSPEND	–	Erase Suspend: Used in conjunction with FAILC/FAIL of the status register (SR[1]/SR[0]) SUSPEND is persistent and will remain set until the Erase Suspend operation is finished after Erase Resume or a RESET (FFh, FAh, FDh) . SUSPEND = 0, FAIL = 0: Erase operation completed with successful status. SUSPEND = 0, FAIL = 1: Erase operation completed with fail status. SUSPEND = 1, FAIL = 0: Erase operation successful suspended SUSPEND = 1, FAIL = 1: This state will exist only for nested suspend: Erase operation suspended successfully. Following Program operation failed. FAILC is valid only in the initial Suspend State (SUSPEND=1) and provides fail status for previous erase immediately completed prior to suspended erase operation FAILC is invalid for any operations performed after suspend is issued and for the Resumed array operation from Suspend State. This bit is valid only when ARDY (SR[5]) or RDY (SR[6]) is 1.
1	FAILC	Yes	Pass/Fail (N–1): 0 = Pass 1 = Fail This bit is set if the program or erase operation (n-1) prior to the currently completed operation (n) on the selected die (LUN) failed. This bit is valid only when ARDY (SR[5]) or RDY (SR[6]) is 1. The valid (n-1) operations for this bit are PROGRAM, COPYBACK PROGRAM, and ERASE-series operations (80h-10h, 80h-15h, 85h-10h, 60h-D0h). This bit is valid following an ERASE-series, PROGRAM-series or READ-series operation (n). This bit is not an indicator for the status of READ-series operations. FAILC is updated if the currently completed operation (n) was a program, read or erase. This bit retains the status of the previous valid program or erase operation (n-1) when the most recent program, read or erase operation (n) is complete. For example, if an erase, program, or read operation (n) is complete and the previous operation (n-1) was a program or erase operation, the FAILC bit will provide pass/fail status information for the previous program or erase operation (n-1).
0	FAIL[5]	Yes	Pass/Fail (N): 0 = Pass 1 = Fail This bit is set if the most recently finished operation on the selected die (LUN) failed. This bit is valid only when ARDY (SR[5]) or RDY (SR[6]) is 1. The valid (n) operations for this bit are PROGRAM, COPYBACK PROGRAM, and ERASE-series operations (80h-10h, 80h-15h, 85h-10h, 60h-D0h). This bit is not valid following a READ-series operation.

Notes: 1. After a multi-plane operation begins, the FAILC and FAIL bits are OR'ed together for the active planes when the READ STATUS (70h) command or FIXED ADDRESS READ STATUS ENHANCED (71h) are issued. After the READ STATUS ENHANCED (78h) command is issued, the FAILC and FAIL bits reflect the status of the plane group selected.
2. In addition to WP# status, SR[7] also provides LOCK Status (SR[7]=0) to indicate the host issued a command that was blocked from execution by the NAND. The LOCK Status is cleared upon the host issuing the next command which includes any program/read/erase command and set/get feature. The LOCK status is Plane independent. If the user issues READ STATUS ENHANCED (78h) to a non-active plane (planes not enabled by user are deemed non-active), then LOCK status (SR[7]) will be invalid.

3. RDY and ARDY have Independent per Plane Group Status Bits during IWL Read. In addition, there will be Die (LUN) level RDY and ARDY status bits. The die (LUN) level RDY will be the AND of the SR[6] values of all plane groups. The die (LUN) level ARDY will be the AND of the SR[5] values of all plane groups. The host will use READ STATUS ENHANCED (78h) to address the required plane group's status register to determine individual plane group status during IWL Read. The READ STATUS (70h) and FIXED ADDRESS READ STATUS ENHANCED (71h) will result in a busy if either of the plane groups are busy. A status value of ARDY = 1 and RDY = 0 may occur as a result of the transition of status signals to other values (ie. ARDY transitions to a '1' faster than RDY transitions to a '1' or RDY transitions to a '0' faster than ARDY transitions to a '0'), but the ARDY = 1 and RDY = 0 status is a transitory value and therefore invalid and shall be ignored by the host. ARDY = 1 is only valid when RDY = 1.
4. SR[4] event could be missed in certain IWL Read conditions. During IWL Read operations, SR[4] = don't care.
5. The FAIL bit is also used during DCC Training and ZQ Calibration (ZQCL, ZQCS) to feedback to the host the pass/fail result of the DCC training or ZQ calibration sequence. After the DCC training or ZQ calibration though, the NAND will remember the FAIL information prior to when the DCC training or ZQ calibration operation was run. For example, if FAIL=1 prior to enabling DCC training via FA:20h P1[0]=1, if DCC training completed successfully then a Read Status while in DCC training mode (FA:20h P1[0]=1) will return FAIL=0, however after the DCC training mode is exited (FA:20h P1[0]=0), a succeeding Read Status will return FAIL=1 which was the previous value of the FAIL bit prior to the DCC training. For a ZQ Calibration operation, if FAIL=1 (due to program failure of Program N-1) prior to the ZQ Calibration operation, then if the ZQ Calibration was successful, a Read Status will return FAIL=0 reflecting that the ZQ Calibration operation was successful, however if a Program N operation is issued immediately afterwards, and Program N was successful, then FAIL=0 (reflecting Program N was successful), but FAILC=1 (reflecting that Program N-1 had failed).

Table 51: Extended Status Register (ESR) Definition

ESR Bit	Definition	Independent per Plane Group	Description
7	Reserved	–	
6	Reserved	–	
5	Reserved	–	
4	Reserved	–	
3	Low V_{CC} Alert	–	Low V_{CC} Alert Status (when enabled): Status = 0: default Status = 1: The NAND will set ESR[3] when V_{CC} is lower than V_{CC} min during an ongoing Read, Program, or Erase operation (e.g. SR[5] = 0). This bit is persistent and must be cleared using Feature Address 84h: Clear Extended Status Register
2	Reserved	–	
1	Thermal Alert High	No	Thermal Alert High Status (when enabled): Status = 0: Temperature is inside the defined temperature range. Status = 1: The NAND will set ESR[1] when the Temperature is higher than the defined temperature range. This bit is persistent and must be cleared using Feature Address 84h: Clear Extended Status Register
0	Thermal Alert Low	No	Thermal Alert Low Status (when enabled): Status = 0: Temperature is inside the defined temperature range. Status = 1: The NAND will set ESR[0] when the Temperature is lower than the defined temperature range. This bit is persistent and must be cleared using Feature Address 84h: Clear Extended Status Register

Table 52: Program Suspend SR[3] and Erase Suspend SR[2] Behavior

Condition	Program Suspend SR[3]	Erase Suspend SR[2]
Only Program Suspended	1	0

Table 52: Program Suspend SR[3] and Erase Suspend SR[2] Behavior (Continued)

Condition	Program Suspend SR[3]	Erase Suspend SR[2]
Read after Program Suspended	1	0
Only Erase Suspended	0	1
Read after Erase Suspended	0	1
Nested Program Suspended	1	1
Read after Nested Program Suspended	1	1
Nested Program Finished/Suspend a Finished Nested Program but Erase still Suspended	0	1

Read Status Restrictions

To avoid bus contention, there are restrictions on READ STATUS (70h) command for all operations with Multi-Lun per CE# packages. READ STATUS (70h) command is target based and it can cause bus contention if used for Multi-Lun per CE# packages.

The host should only use EXTENDED STATUS REGISTER READ (79h) command after READ STATUS (70h), FIXED ADDRESS READ STATUS ENHANCED (71h), or READ STATUS ENHANCED (78h) command to determine event that triggered SR[4] high.

Table 53: Status Command Use After Initial Operation

Initial Operation	READ STATUS (70h)	FIXED ADDRESS READ STATUS ENHANCED (71h)	READ STATUS ENHANCED (78h)	EXTENDED STATUS REGISTER READ (79h)
Array or Algo Command	Multi-LUN per CE: No	Yes	Yes	Yes [1]
	Single LUN per CE: Yes			

Notes: 1. EXTENDED STATUS REGISTER READ (79h) can be used after SR[4]=1 to determine cause of ESR flag bit = 1.

READ STATUS (70h)

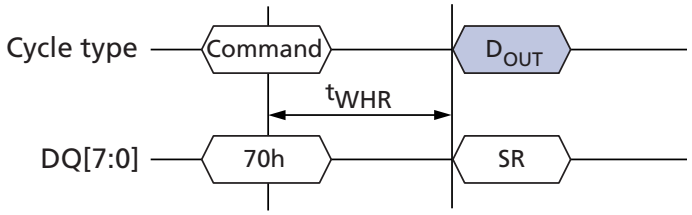
The READ STATUS (70h) command returns the status of the last-selected die (LUN) on a target. This command is accepted by the last-selected die (LUN) even when it is busy (RDY = 0).

If there is only one die (LUN) per target, the READ STATUS (70h) command can be used to return status following any NAND command.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select the die (LUN) that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as two or more die (LUNs) could respond until the next operation is issued. The READ STATUS (70h) command can be used following all single die (LUN) operations.

If following a multi-plane operation, regardless of the number of LUNs per target, the READ STATUS (70h) command indicates an error occurred (FAIL = 1), use the READ STATUS ENHANCED (78h) command—once for each plane—to determine which plane operation failed.

Figure 63: READ STATUS (70h) Operation



READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed plane on the selected die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0).

Writing 78h to the command register, followed by address cycle input containing the page, block, and LUN addresses, puts the selected plane into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

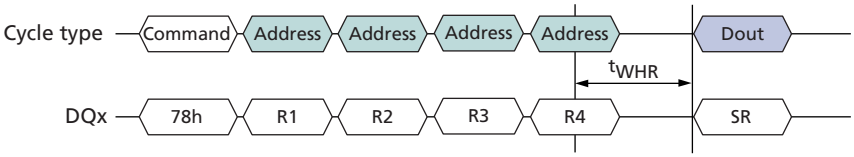
The selected LUN's status is returned when the host requests data output. The FAILC and FAIL bits are specific to the plane specified in the row address. The RDY and ARDY bits of the status register are unique for each plane group of the selected die (LUN) when doing IWL Read.

The READ STATUS ENHANCED (78h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command after the die (LUN) is ready (see CHANGE READ COLUMN ENHANCED (06h-E0h)).

Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET (FFh) command and when OTP mode is enabled. It is also prohibited following some of the other reset, identification, and configuration operations. See individual operations for specific details.

See the Interleaved Die (Multi-LUN) Operations section for data output requirements for interleaving operations between multiple die (LUNs).

Figure 64: READ STATUS ENHANCED (78h) Operation



FIXED ADDRESS READ STATUS ENHANCED (71h)

The FIXED ADDRESS READ STATUS ENHANCED (71h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0). The FIXED ADDRESS READ STATUS ENHANCED (71h) command returns status output in the same manner as the READ STATUS (70h) command.

Use of the FIXED ADDRESS READ STATUS ENHANCED (71h) command is allowed during the power-on RESET (FFh) command (during tPOR) and when OTP mode is enabled. It is also allowed following some of the other reset, identification, and configuration operations that READ STATUS ENHANCED (78h) is prohibited.

Writing 71h to the command register, followed by one row address cycle containing the hardcoded LUN selection, puts the selected die (LUN) into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

The selected LUN's status is returned when the host requests data output. The RDY, ARDY, FAILC and FAIL bits of the status register are shared for all of the planes of the selected die (LUN).

The FIXED ADDRESS READ STATUS ENHANCED (71h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY=1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the CHANGE READ COLUMN ENHANCED (06h-E0h, 00h-05h-E0h) command after the die (LUN) is ready (see CHANGE READ COLUMN ENHANCED (06h-E0h, 00h-05h-E0h)).

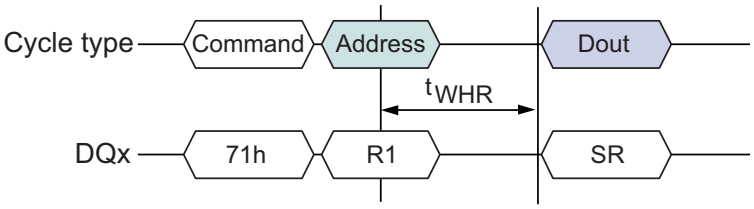
See the Interleaved Die (Multi-LUN) Operations section for data output requirements for interleaving operations between multiple die (LUNs).

Table 54: R1 Address Cycle Decoding for 71h Operation

Description	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
R1											
Bits LA0 (DQ0) and LA1 (DQ1) for LUN selection	LUN0							0	0	00b	
	LUN1							0	1	01b	
	LUN2							1	0	10b	
	LUN3							1	1	11b	
Reserved	Don't Care	-	-	-	-	-	-			-	1

Notes: 1. Can be either '1' or '0'.

Figure 65: FIXED ADDRESS READ STATUS ENHANCED (71h) Operation



EXTENDED STATUS REGISTER READ (79h)

The EXTENDED STATUS REGISTER READ (79h) command returns the Extended Status Register (ESR) of the addressed plane on the selected die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0).

Writing 79h to the command register, followed by address cycle input containing the page, block, and LUN addresses, puts the selected plane into extended read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

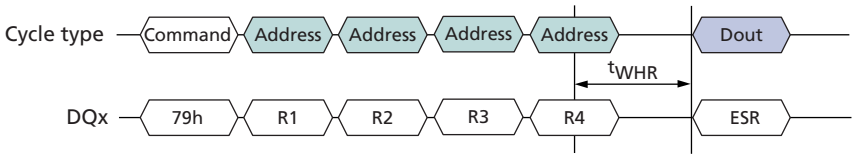
The selected LUN's Extended Status is returned when the host requests data output. All bits of the Extended Status Register are specific to the selected die (LUN).

The host should only use EXTENDED STATUS REGISTER READ (79h) command after READ STATUS (70h), FIXED ADDRESS READ STATUS ENHANCED (71h), or READ STATUS ENHANCED (78h) command to determine event that triggered SR[4] high.

The EXTENDED STATUS REGISTER READ (79h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command after the die (LUN) is ready (see CHANGE READ COLUMN ENHANCED (06h-E0h)).

Use of the EXTENDED STATUS REGISTER READ (79h) command is prohibited during the power-on RESET (FFh) command and when OTP mode is enabled. It is also prohibited following some of the other reset, identification, and configuration operations. See individual operations for specific details.

Figure 66: EXTENDED STATUS REGISTER READ (79h) Operation



Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the selected die (LUNs). These features provide host flexibility for managing data, especially when the host internal buffer is smaller than the number of data bytes or words in the cache register.

In synchronous interface, column address operations are aligned to word boundaries (CA0 is forced to 0), because as data is transferred on DQ[7:0] in two-byte units.

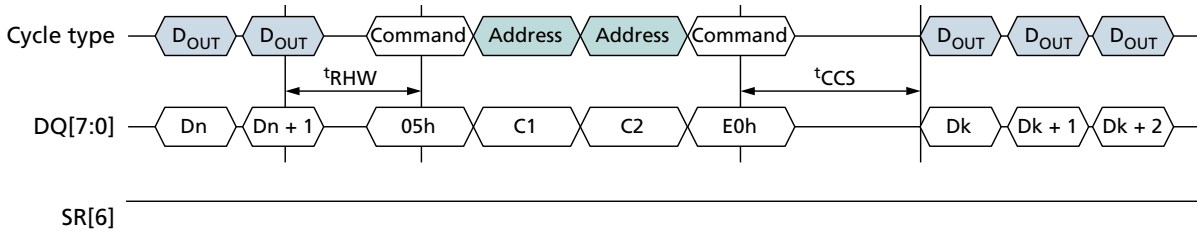
CHANGE READ COLUMN (05h-E0h)

The CHANGE READ COLUMN (05h-E0h) command changes the column address of the selected cache register and enables data output from the last selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE operations (RDY = 1; ARDY = 0) but is limited to CACHE READ. CACHE PROGRAM is not allowed.

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the selected die (LUN) into data output mode. After the E0h command cycle is issued, the host must wait at least ^{t}CCS before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be issued prior to issuing the CHANGE READ COLUMN (05h-E0h). In this situation, using the CHANGE READ COLUMN (05h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

Figure 67: CHANGE READ COLUMN (05h-E0h) Operation



CHANGE READ COLUMN ENHANCED (06h-E0h)

The CHANGE READ COLUMN ENHANCED (06h-E0h) command enables data output on the addressed die's (LUN's) cache register at the specified column address. This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE operations (RDY = 1; ARDY = 0) but is limited to CACHE READ. CACHE PROGRAM is not allowed.

Writing 06h to the command register, followed by the required address cycle input, followed by E0h, enables data output mode on the address LUN's cache register at the specified column address. Only the column, plane and LUN addresses are valid; the page and block addresses are ignored. After the E0h command cycle is issued, the host must wait at least ^{t}CCS before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

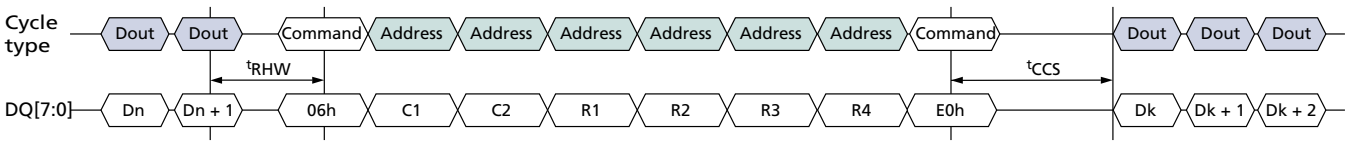
Following a MULTI-PLANE READ PAGE operation, the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select the cache register to be enabled for data output. After data output is complete on the selected plane, the command can be issued again to begin data output on another plane.

In devices with more than one die (LUN) per target, after all of the die (LUNs) on the target are ready (RDY = 1), the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used following an interleaved die (multi-LUN) READ operation. Die (LUNs) that are not addressed are deselected to avoid bus contention.

In devices with more than one die (LUN) per target, during interleaved die (multi-LUN) operations where more than one or more die (LUNs) are busy (RDY = 1; ARDY = 0 or RDY = 0; ARDY = 0), the READ STATUS ENHANCED (78h) command must be issued to the die (LUN) to be selected prior to issuing the CHANGE READ COLUMN ENHANCED (06h-E0h). In this situation, using the CHANGE READ COLUMN ENHANCED (06h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

If there is a need to update the column address without selecting a new cache register or LUN, the CHANGE READ COLUMN (05h-E0h) command can be used instead.

Figure 68: CHANGE READ COLUMN ENHANCED (06h-E0h) Operation

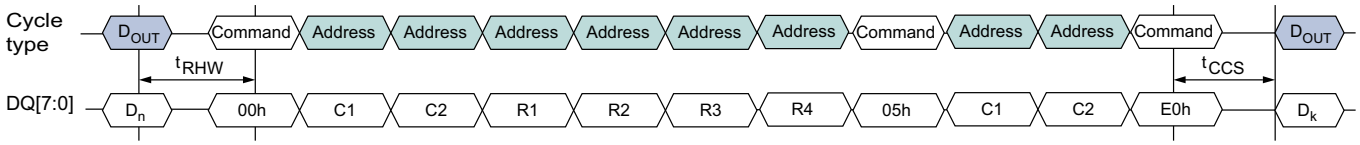


CHANGE READ COLUMN ENHANCED (00h-05h-E0h)

This operation behaves the same as the CHANGE READ COLUMN ENHANCED (06h-E0h) command.

If a 00h command is issued to a LUN followed by address cycle input and no valid subsequent confirm command for that operation is issued (that is, 05h, 20h, 30h, 31h, 32h, 34h, 35h, etc), a RESET (FFh, FAh) command is required before another 00h command can be issued to that LUN to start a new read operation sequence, or to start that LUN's read operation over without executing that operation (that is, repeating or changing Address Cycle input again).

Figure 69: CHANGE READ COLUMN ENHANCED (00h-05h-E0h) Operation



CHANGE WRITE COLUMN (85h)

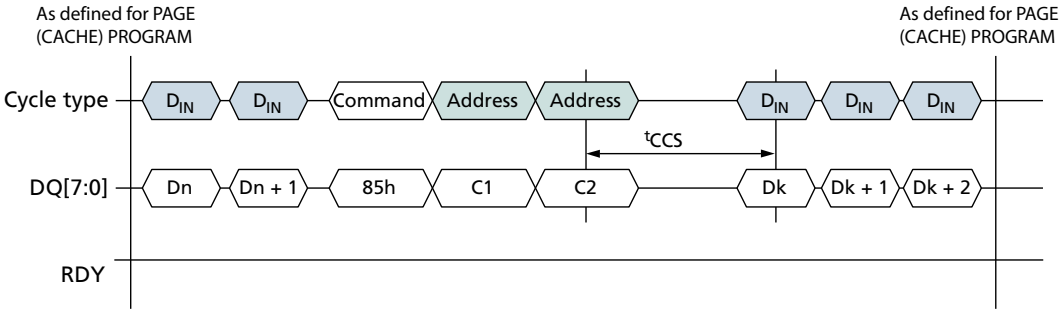
The CHANGE WRITE COLUMN (85h) command changes the column address of the selected cache register and enables data input on the last-selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE PROGRAM operations
(RDY = 1; ARDY = 0).

Writing 85h to the command register, followed by two column address cycles containing the column address, puts the selected die (LUN) into data input mode. After the second address cycle is issued, the host must wait at least ^{t}CCS before inputting data. The selected die (LUN) stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE WRITE COLUMN (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h).

In devices that have more than one die (LUN) per target, the CHANGE WRITE COLUMN (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

Figure 70: CHANGE WRITE COLUMN (85h) Operation



CHANGE ROW ADDRESS (85h)

The CHANGE ROW ADDRESS (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND Flash array. It also changes the column address of the selected cache register and enables data input on the specified die (LUN). This

command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE PROGRAMMING operations (RDY = 1; ARDY = 0).

Write 85h to the command register. Then issue the required address cycle input. This updates the page and block destination of the selected plane for the addressed LUN and puts the cache register into data input mode. After the required address cycles have been issued the host must wait at least ^{t}CCS before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE ROW ADDRESS (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h). When used with these commands, the LUN address and plane select bits are required to be identical to the LUN address and plane select bits originally specified.

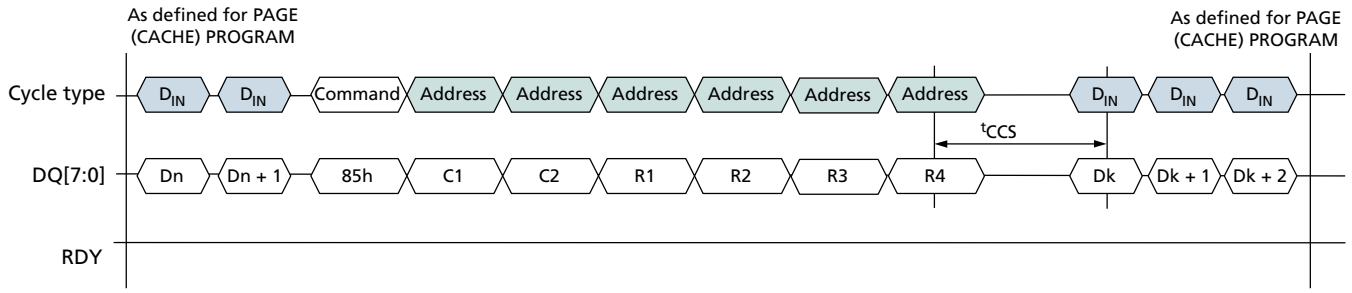
The CHANGE ROW ADDRESS (85h) command enables the host to modify the original page and block address for the data in the cache register to a new page and block address.

In devices that have more than one die (LUN) per target, the CHANGE ROW ADDRESS (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

The CHANGE ROW ADDRESS (85h) followed by an 11h command can be used with the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) commands to read and modify cache register contents in small sections prior to programming cache register contents to the NAND Flash array. This capability can reduce the amount of buffer memory used in the host controller.

To modify the cache register contents in small sections, first issue a PAGE READ (00h-30h) or COPYBACK READ (00h-35h) operation. When data output is enabled, the host can output a portion of the cache register contents. To modify the cache register contents, issue the 85h command, the column and row addresses, and input the new data. The host can re-enable data output by issuing the 11h command, waiting ^{t}DBSY, and then issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h / 00h-05h-E0h) command. It is possible to toggle between data output and data input multiple times by re-issuing an 11h command prior to data output commands. After the final CHANGE ROW ADDRESS (85h) operation is complete, issue the 10h command to program the cache register to the NAND Flash array.

Figure 71: CHANGE ROW ADDRESS (85h) Operation



Read Operations

Read operations are used to read data from the NAND Flash array of one or more of the planes to their respective cache and/or data registers for data output.

This device may provide cache register availability before the entire read operation is complete. Status Register bit 6 ('RDY') will provide a method for the host to determine when data can begin being clocked out of the device. The host may begin clocking data out of the device when SR[6] goes HIGH. This reduces the apparent ^{t}R time for Read operations. Status Register bit 5 ('ARDY') will remain LOW until the entire read algorithm has been completed. The host must not issue any additional operations until SR[5] is HIGH with these exceptions.

- This functionality may not be available during READ UNIQUE ID (EDh), READ PARAMETER PAGE (ECh), and SINGLE BIT SOFT BIT READ PAGE (00h-34h).
- See IWL READ (00h-20h) section for restrictions during IWL READ operation.
- During the time that cache register is available at the end of the read but the entire read operation is not complete (RDY = 1, ARDY = 0) only the following commands will be accepted by the NAND device: READ STATUS (70h/71h/78h), RESET (FFh/FAh), CHANGE READ COLUMN (05h-E0h), CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h), READ PAGE CACHE SEQUENTIAL (31h), READ PAGE CACHE RANDOM (00h-31h), READ PAGE CACHE LAST (3Fh), READ PAGE MULTI-PLANE (00h-32h), READ PAGE (00h-30h), READ MODE (00h).

Table 55: Read Operations with ^{t}R Reduction Functionality

Read operation	^{t}RTABSY[1] applies
Regular Read (including Read Page, IWL, ARC, ACRR, Read Offsets)	YES
SBSBR	YES
Read OTP page	YES
Cache Read exit 3Fh	NO
Read Unique ID	NO
Read Parameter Page	NO

Notes: 1. Busy time for read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array read operation.

If a 00h command is issued to a LUN followed by address cycle input and no valid subsequent confirm command for that operation is issued (that is, 05h, 20h, 30h, 31h, 32h, 34h, 35h, etc), a RESET (FFh, FAh) command is required before another 00h command can be issued to that LUN to start a new read operation sequence, or to start that LUN's read operation over without executing that operation (that is, repeating or changing Address Cycle input again).

Read Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND Flash array to its cache register and enables data output for that cache register.

The READ MODE (00h) command enables data output for the last-selected die (LUN) and cache register. The READ MODE (00h) command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1 or 0) following a READ operation, status operations following a READ operation, CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h / 00h-05h-E0h) command.

After a READ operation, the READ MODE (00h) command disables status output and enables data output for the last-selected die (LUN) and cache register has been monitored with a status operation (70h, 71h, 78h).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command must be used to select only one die (LUN) prior to issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h / 00h-05h-E0h) to enable data output to prevent bus contention.

Read Cache Operations

To increase data throughput, the READ PAGE CACHE-series (31h, 00h-31h, 3Fh) commands can be used to output data from the cache register while concurrently reading a page from the NAND Flash array to the data register.

To begin a read page cache sequence, begin by reading a page from the NAND Flash array to its corresponding cache register using the READ PAGE (00h-30h) command. During ^{t}R, R/B# goes LOW and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After ^{t}R, R/B# goes HIGH and the selected die (LUN) is ready (RDY = 1, ARDY = 1 or 0), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h)—reads the next sequential page from the NAND Flash array to the data register
- READ PAGE CACHE RANDOM (00h-31h)—reads the page specified in this command from the NAND Flash array (any plane) to its corresponding data register

After the READ PAGE CACHE-series (31h, 00h-31h) commands have been issued, R/B# goes LOW and the selected die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY1 or ^{t}RCBSY2. After ^{t}RCBSY1 or ^{t}RCBSY2, R/B# goes HIGH and the selected die (LUN) is ready (RDY = 1, ARDY = 1 or 0). The cache register becomes available and the page requested in the READ PAGE CACHE operations is transferred to the data register. At this point, data can be output from the cache register, beginning at column address 0 (if issuing the 31h command) or the addressed column address (if issuing the 00h-31h command). The CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command can be used to change the column address of the data being output.

To end a READ PAGE CACHE SEQUENTIAL (31h) or READ PAGE CACHE RANDOM (00h-31h) sequence, a READ PAGE CACHE LAST (3Fh) command must be issued. When the READ PAGE CACHE LAST (3Fh) command is issued, RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY1 or ^{t}RCBSY2 while the data register is copied into the cache register. After ^{t}RCBSY1 or ^{t}RCBSY2, R/B# goes HIGH, indicating that the cache register is available and the die (LUN) is ready. Data can then be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY1 or ^{t}RCBSY2, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 71h, 78h) and RESET (FFh, FAh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status operations (70h, 71h, 78h), READ MODE (00h), READ PAGE CACHE-series (31h, 00h-31h, 3Fh), READ PAGE MULTI-PLANE (00h-32h), CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) and RESET (FFh, FAh).

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with READ PAGE CACHE LAST (3Fh) command. A READ PAGE CACHE LAST (3Fh) command is required to be issued to close out a cache read command sequence.

Multi-Plane Read Operations

Multi-plane read page operations improve data throughput by reading data from more than one plane simultaneously to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the READ PAGE (00h-30h) command.

When the die (LUN) is ready, the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command determines which plane outputs data. During data output, the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h). See Multi-Plane Operations for details.

Multi-Plane Read Cache Operations

Multi-plane read cache operations can be used to output data from more than one cache register while concurrently reading one or more pages from more than one plane simultaneously to the data register. This is done by prepending READ PAGE MULTI-PLANE (00h-32h) commands in front of the PAGE READ CACHE RANDOM (00h-31h) command.

To begin a multi-plane read page cache sequence, begin by issuing the READ PAGE MULTI-PLANE (00h-32h) command and READ PAGE (00h-30h) commands. During ^{t}DBSY or ^{t}R, R/B# goes LOW and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After ^{t}DBSY or ^{t}R, R/B# goes HIGH and selected die is ready (RDY = 1, ARDY = 1 or 0), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h)—reads the next sequential page from the previously addressed planes from the NAND Flash array to the data registers
- READ PAGE MULTI-PLANE (00h-32h) commands, if desired, followed by the READ PAGE CACHE RANDOM (00h-31h) command—reads the pages specified from the NAND Flash array to the corresponding data registers

After the READ PAGE CACHE series (31h, 00h-31h) commands have been issued, R/B# goes LOW and the selected die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY1 or ^{t}RCBSY2. After ^{t}RCBSY1 or ^{t}RCBSY2, R/B# goes HIGH and the selected die (LUN) is ready (RDY = 1, ARDY = 1 or 0). The cache register becomes available and the page requested in the READ PAGE CACHE operations is transferred to the data register. After ^{t}RCBSY1 or ^{t}RCBSY2, R/B# goes HIGH and the LUN's status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache registers become available and the pages requested in the READ PAGE CACHE operation are transferred to the data registers. Issue the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command to determine which cache register will output data. After data is output, the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the CHANGE READ COLUMN (05h- E0h) command can be used to change the column address of the data output.

After outputting data from the cache registers, an additional MULTI-PLANE READ CACHE-series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued. To end a multi-plane read page cache sequence, a READ PAGE CACHE LAST (3Fh) must be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY1 or ^{t}RCBSY2 while the data registers are copied into the cache registers. After tRCBSY1 or ^{t}RCBSY2, R/B# goes HIGH, indicating that the cache registers are available and that the die (LUN) is ready. Issue the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command to determine which cache register will output data. After data is output, the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY1 or ^{t}RCBSY2, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 71h, 78h)

and RESET (FFh, FAh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status operations (70h, 71h, 78h), READ MODE (00h), READ PAGE CACHE-series (31h, 00h-31h, 3Fh), READ PAGE MULTI-PLANE (00h-32h), CHANGE READ COLUMN (05h-E0h), CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) and RESET (FFh, FAh).

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with READ PAGE CACHE LAST (3Fh) command.

See Multi-Plane Operations for additional multi-plane addressing requirements.

Valid Commands during Read Operations

There are certain commands that will be accepted by the NAND device during various read operations when die (LUN) is busy (RDY = 0, ARDY = 0) and when die (LUN) is ready (RDY = 1, ARDY = 0). During ^{t}R, ^{t}RCBSY1 or ^{t}RCBSY2, and ^{t}DBSY for read operations, when the die (LUN) is busy (RDY = 0, ARDY = 0), the only valid commands are RESET (FFh/FAh) and READ STATUS (70h/71h/78h).

After ^{t}R, ^{t}RCBSY1 or ^{t}RCBSY2, and ^{t}DBSY for read operations, when the die (LUN) is ready (RDY = 1, ARDY = 0), the valid commands are shown in the following table:

Table 56: Only Valid Commands when die (LUN) is Ready (RDY = 1, ARDY = 0) for READ PAGE (00h-30h), READ PAGE CACHE-series (31h, 00h-31h, 3Fh), and READ PAGE MULTI-PLANE (00h-32h)

Commands	READ PAGE (00h-30h)	READ PAGE CACHE-Series (31h, 00h-31h, 3Fh)	READ PAGE MULTI-PLANE (00h-32h)
RESET (FFh/FAh)	Valid	Valid	Valid
READ STATUS (70h/71h/78h)	Valid	Valid	Valid
CHANGE READ COLUMN (05h-E0h)	Valid	Valid	Valid
CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h)	Valid	Valid	Valid
READ MODE (00h)	Valid	Valid	Valid
READ PAGE (00h-30h)	Valid	Not valid	Not valid
READ PAGE CACHE SEQUENTIAL (31h)	Valid	Valid	Not valid
READ PAGE CACHE RANDOM (00h-31h)	Valid	Valid	Valid
READ PAGE CACHE LAST (3Fh)	Valid	Valid	Not valid
READ PAGE MULTI-PLANE (00h-32h)	Valid	Valid	Valid
SET FEATURES	Not valid	Not valid[1]	Not valid
READ OFFSET PREFIX (2Eh)	Valid	Valid	Valid
SLC MODE LUN ENABLE (3Bh)	Valid	Valid	Valid

Notes: 1. See READ OFFSET PREFIX COMMAND (2Eh) for setting Read Verify level.

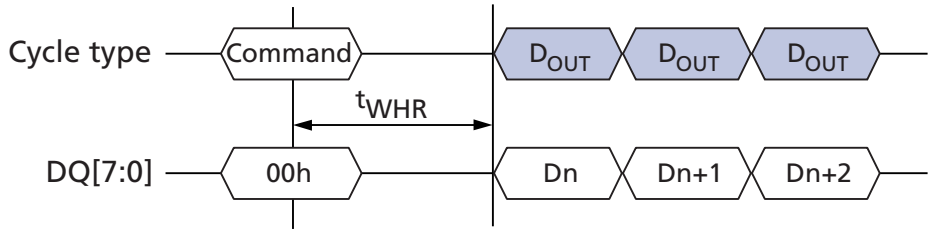
READ MODE (00h)

The READ MODE (00h) command enables data output for the last-selected die (LUN) and cache register. The READ MODE (00h) command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1 or 0) following a READ operation, status operations following a READ operation, CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h / 00h-05h-E0h) command.

After a READ operation, the READ MODE (00h) command disables status output and enables data output for the last-selected die (LUN) and cache register that has been monitored with a status operation (70h, 71h, 78h).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command must be used to select only one die (LUN) prior to issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h / 00h-05h-E0h) to enable data output to prevent bus contention.

Figure 72: READ MODE (00h) Operation



READ PAGE (00h-30h)

The READ PAGE (00h–30h) command reads a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1 or 0).

To read a page from the NAND Flash array, issue 00h to the command register, then write the required address cycles to the address register, and conclude with 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}R as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h/71h/78h) can be used. If the status operations are used to monitor the LUN's status, when the die (LUN) is ready (RDY = 1, ARDY = 1 or 0), the READ MODE (00h) command can be issued to disable status output and enable data output. When the host requests data output, output begins at the column address specified.

During data output, the CHANGE READ COLUMN (05h-E0h) command or the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command can be used to change the column address of the data being output from the cache register.

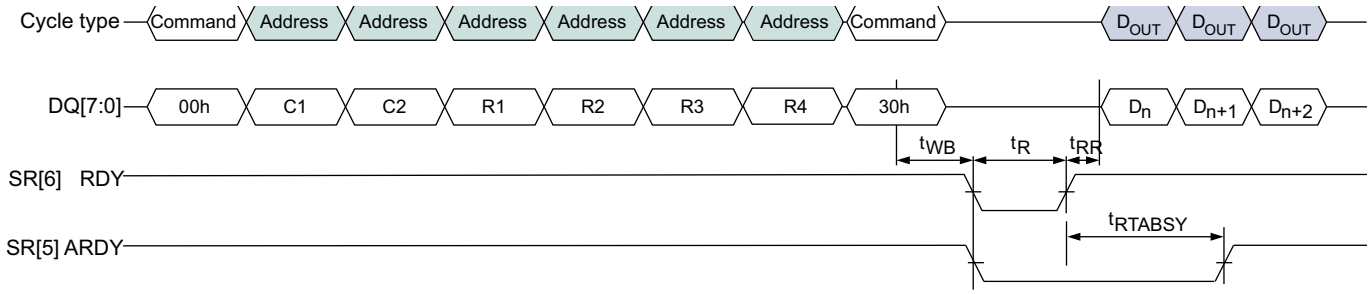
The READ PAGE (00h-30h) command cannot be issued to a LUN when its status bit SR[5] (ARDY) = 1.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command must be used to select only one die (LUN) prior to issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h / 00h-05h-E0h) to enable data output to prevent bus contention.

The READ PAGE (00h-30h) command is used as the final command of a multi-plane read operation. It is preceded by one or more READ PAGE MULTI-PLANE (00h-32h) commands. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1 or 0), data output is enabled for the cache register linked to the least significant plane addressed, regardless of input order. When the host requests data output, output begins at the column address last specified in the READ PAGE (00h-30h) command. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED

(06h-E0h/00h-05h-E0h) command. See Multi-Plane Operations for additional multi-plane addressing requirements.

Figure 73: READ PAGE (00h-30h) Operation



READ PAGE CACHE SEQUENTIAL (31h)

The READ PAGE CACHE SEQUENTIAL (31h) command reads the next sequential page into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1 or 0).

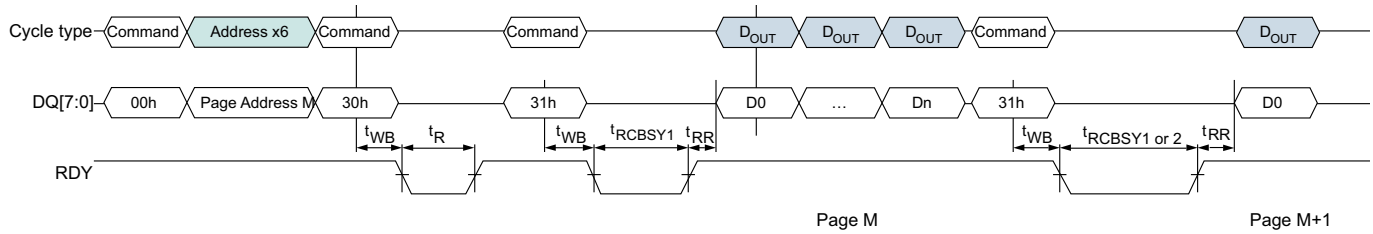
To read the next sequential page, issue 31h to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for tRCBSY1 or tRCBSY2. After tRCBSY1 or tRCBSY2, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is reading from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command or the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command can be used to change the column address of the data being output from the cache register.

The READ PAGE CACHE SEQUENTIAL (31h) command can be used to cross block boundaries. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a block is read into the data register, the next page read will be the next logical block in the plane which the 31h command was issued. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a plane is read into the data register, the NAND device will keep outputting the data from the last page of the plane. The last page of the plane is not re-read from the NAND array. Data is kept in the cache register and read from there. Do not issue the READ PAGE CACHE SEQUENTIAL (31h) to cross die (LUN) boundaries. Instead, issue the READ PAGE CACHE LAST (3Fh) command.

If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after a MULTI-PLANE READ PAGE operation (00h-32h, 00h-30h), the next sequential pages are read into the data registers while the previous pages can be output from the cache registers. During multi-plane sequential cache read mode, if the READ PAGE CACHE SEQUENTIAL (31h) command is issued after reading the last page in the last block in one plane and a last page in a random block in the other plane, the circuit increments the block address and page address for only the plane that has not reached the end of its plane addressing. After the die (LUN) is ready (RDY = 1, ARDY = 1 or 0), the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command is used to select which cache register outputs data.

A READ PAGE CACHE LAST (3Fh) command is required to be issued to close out a cache read command sequence.

Figure 74: READ PAGE CACHE SEQUENTIAL (31h) Operation



READ PAGE CACHE RANDOM (00h-31h)

The READ PAGE CACHE RANDOM (00h-31h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1 or 0).

To read the specified block and page into the data register, issue 00h to the command register, then write the required address cycles to the address register, and conclude with 31h command. The column address in the address specified is ignored. The die (LUN) address must match the same die (LUN) address as the previous READ PAGE (00h-30h) command or, if applicable, the previous READ PAGE CACHE RANDOM (00h-31h) command. There is no restriction on the plane address.

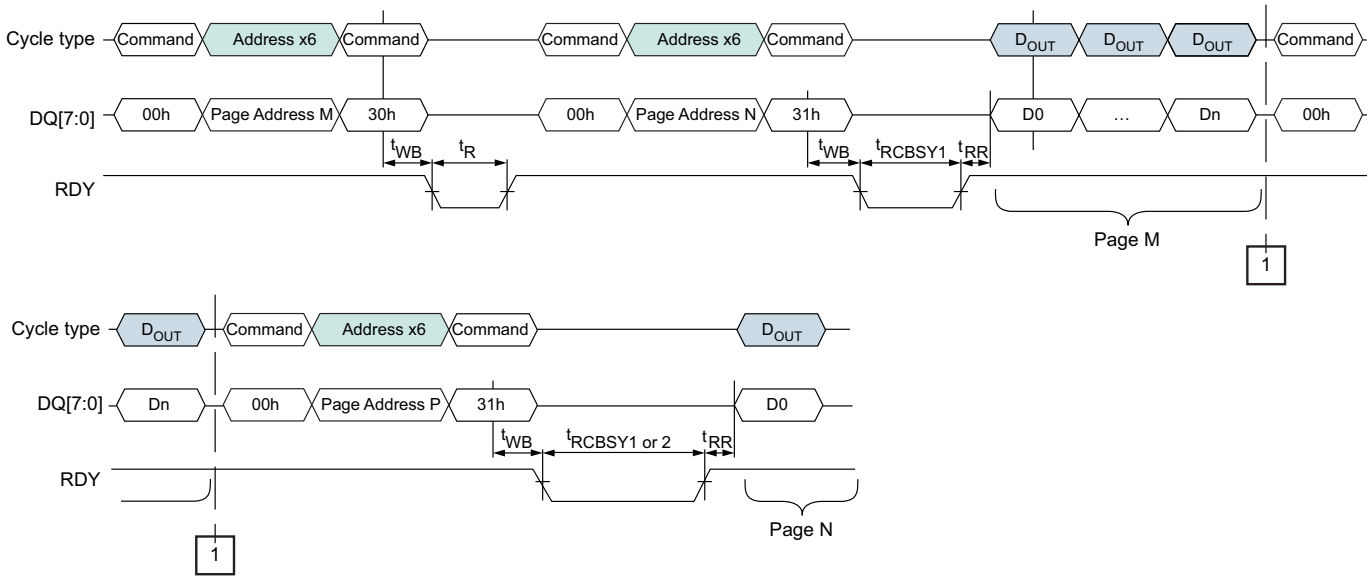
After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY1 or ^{t}RCBSY2. After ^{t}RCBSY1 or ^{t}RCBSY2, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is reading from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command or the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command must be used to select only one die (LUN) prior to issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h / 00h-05h-E0h) to enable data output to prevent bus contention.

If a MULTI-PLANE CACHE RANDOM (00h-32h, 00h-31h) command is issued after a MULTI-PLANE READ PAGE operation (00h-32h, 00h-30h), then the addressed pages are read into the data registers while the previous pages can be output from the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 1 or 0), the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command is used to select which cache register outputs data.

A READ PAGE CACHE LAST (3Fh) command is required to be issued to close out a cache read command sequence.

Figure 75: READ PAGE CACHE RANDOM (00h-31h) Operation



READ PAGE CACHE LAST (3Fh)

The READ PAGE CACHE LAST (3Fh) command ends the read page cache sequence and copies a page from the data register to the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1 or 0).

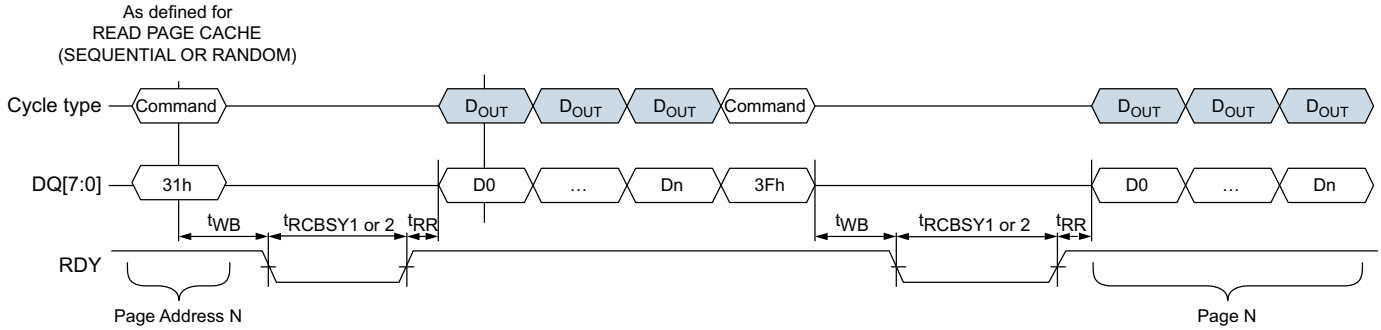
To end the read page cache sequence, issue 3Fh to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY1 or ^{t}RCBSY2. After ^{t}RCBSY1 or ^{t}RCBSY2, R/B# goes HIGH and the die (LUN) is ready. At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command or the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command must be used to select only one die (LUN) prior to issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h / 00h-05h-E0h) to enable data output to prevent bus contention.

If the READ PAGE CACHE LAST (3Fh) command is issued after a MULTI-PLANE READ PAGE CACHE operation (31h, 00h-31h, 00h-32h, 00h-30h), the die (LUN) goes busy until the pages are copied from the data registers to the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 1 or 0), the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command is used to select which cache register outputs data.

A READ PAGE CACHE LAST (3Fh) command is required to be issued to close out a cache read command sequence.

Figure 76: READ PAGE CACHE LAST (3Fh) Operation



READ PAGE MULTI-PLANE (00h-32h)

The READ PAGE MULTI-PLANE (00h-32h) command queues a plane to transfer data from the NAND flash array to its cache register. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for data transfer. The READ PAGE (00h-30h) command is issued to select the final plane and to begin the read operation for all previously queued planes.

To issue the READ PAGE MULTI-PLANE (00h-32h) command, issue 00h to the command register, then write the required address cycles to the address register, and conclude with 32h command. The column address in the address specified is ignored.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}DBSY. After ^{t}DBSY, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1 or 0). At this point, the die (LUN) and block are queued for data transfer from the array to the cache register for the addressed plane.

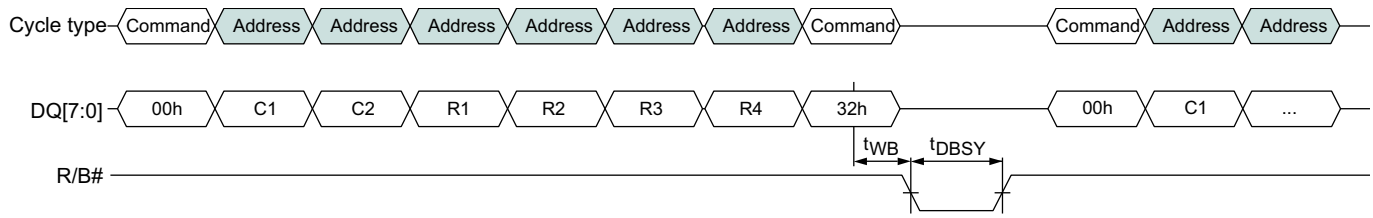
Additional READ PAGE MULTI-PLANE (00h-32h) commands can be issued to queue additional planes for data transfer.

If the READ PAGE (00h-30h) command is used as the final command of a MULTI-PLANE READ operation, data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1 or 0), data output is enabled for the cache register linked to the least significant plane addressed, regardless of input order. When the host requests data output, it begins at the column address specified in the READ PAGE (00h-30h) command. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

If the READ PAGE CACHE SEQUENTIAL (31h) is used as the final command of a MULTI-PLANE READ CACHE operation, data is read from the previously read operation from each plane to each cache register and then data is transferred from the NAND Flash array for all previously addressed planes to their respective data registers. If the READ PAGE CACHE RANDOM (00h-31h) command is used as the final command of a MULTI-PLANE READ CACHE operation, data is read from the previously read operation from the data register to the cache register and then data is transferred from the NAND Flash array for all of the addressed planes to their respective data registers. When the die (LUN) is ready (RDY = 1, ARDY = 1 or 0), data output is enabled. The CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command can be used to determine which cache register outputs data first, and to enable data output in the other cache registers. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

See Multi-Plane Operations for additional multi-plane addressing requirements.

Figure 77: READ PAGE MULTI-PLANE (00h-32h) Operation



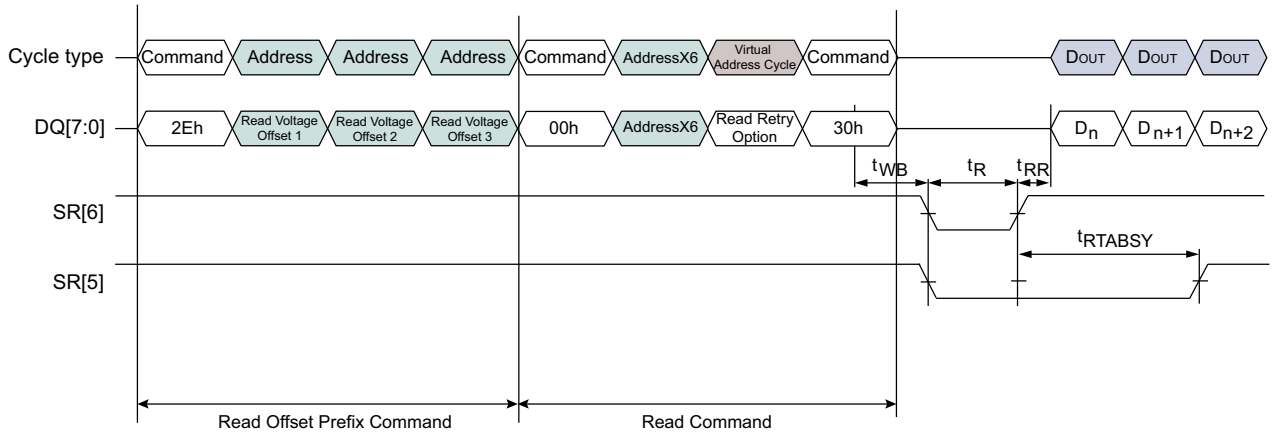
READ OFFSET PREFIX (2Eh) Command

This feature allows the host to quickly apply read offsets to a read without having to use Feature Addresses. The READ OFFSET PREFIX (2Eh) Command offers improved Quality of Service when servicing high priority reads by the system.

Read Offset Prefix Concept

The Read Offset Prefix sequence allows the host to apply read offset levels to a subsequent read operation by issuing a prefix prior to that read. The Read Offset Prefix command sequence consists of the 2Eh command followed by 3 offset cycles.

Figure 78: READ OFFSET PREFIX (2Eh) Command with Read Page (00h-30h) with ACRR Enabled



Based on the page type (LP, UP, XP) of the subsequent read operation, the offsets are interpreted as the appropriate read levels for that read. If the subsequent read does not require 3 read levels (Ex: LP, XP, SLC page reads) then the unused offsets need to be set to 00h.

Table 57: Offset Cycle Encoding

Page Type	Cycle 1	Cycle 2	Cycle 3
SLC	rSLC/rSLC_edge	00h	00h
MLC LP	rL2_2bpc	00h	00h
MLC UP	rL1_2bpc	rL3_2bpc	00h
TLC LP	rL1_3bpc	rL5_3bpc	00h
TLC UP	rL2_3bpc	rL4_3bpc	rL6_3bpc
TLC XP	rL3_3bpc	rL7_3bpc	00h

Once the read level offsets are entered via the prefix command sequence, they are persistent and will be applied to all subsequent reads of that page type (Lower Page, Upper Page, eXtra Page, SLC, or MLC pages), even when the prefix command sequence is not issued.

The last valid read offsets applied via the READ OFFSET PREFIX (2Eh) Command are stored in Feature Addresses A0h-ABh and can be read out by the host with a Get Features by LUN command. Changing the offsets stored in Feature Addresses A0h-ABh via Set Features by LUN command is not allowed.

Example Sequences

TLC Shared Page Reads

When trying to apply a read offset to TLC Shared Page Read the sequence the host would have to issue it as follows.

Lower Page Read Sequence
1. 2Eh: [Offset1(rL1_3bpc), Offset2 (rL5_3bpc), Offset3 (00h)] // Read Offset Prefix Command
2. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 30h // LP Page Read

Upper Page Read Sequence
1. 2Eh: [Offset1(rL2_3bpc), Offset2 (rL4_3bpc), Offset3 (rL6_3bpc)] // Read Offset Prefix Command
2. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 30h // UP Page Read

eXtra Page Read Sequence
1. 2Eh: [Offset1(rL3_3bpc),Offset2 (rL7_3bpc), Offset3 (00h)] // Read Offset Prefix Command
2. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 30h // XP Page Read

MLC Shared Page Reads

When trying to apply a read offset to MLC Shared Page Read(in a TLC Block) the sequence the host would have to issue it as follows.

Lower Page Read Sequence
1. 2Eh: [Offset1(rL2_2bpc), Offset2 (00h), Offset3 (00h)] // Read Offset Prefix Command
2. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 30h // LP Page Read

Upper Page Read Sequence
1. 2Eh: [Offset1(rL1_2bpc), Offset2 (rL3_2bpc), Offset3 (00h)] // Read Offset Prefix Command
2. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 30h // UP Page Read

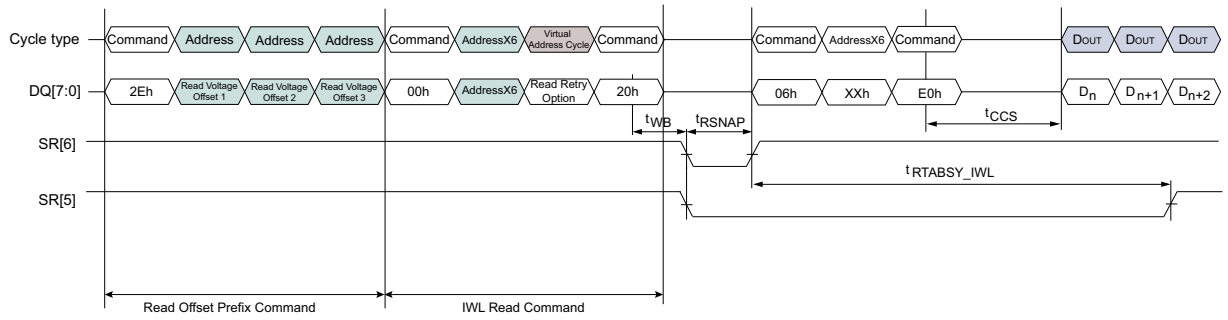
SLC Edge Page Reads

When trying to apply a read offset to SLC Edge Page Read(in a TLC Block) the sequence the host would have to issue it as follows.

Lower Page Read Sequence
1. 2Eh: [Offset1(rSLC_edge), Offset2 (00h), Offset3 (00h)] // Read Offset Prefix Command
2. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 30h // SLC Page Read

The READ OFFSET PREFIX (2Eh) Command can also be used in conjunction with IWL READ (00h-20h). The sequence and implementation are identical to the examples shown above for PAGE READ (00h-30h). IWL READ can only be used where all shared pages have been programmed.

Figure 79: READ OFFSET PREFIX (2Eh) Command with IWL READ (00h-20h) with ACRR Enabled



Example Sequences

TLC Shared Page IWL Read

When trying to apply a read offset to TLC Shared Page IWL Read the sequence the host would have to issue it as follows.

Lower Page IWL Read Sequence

1. 2Eh: [Offset1(rL1_3bpc), Offset2 (rL5_3bpc), Offset3 (00h)] // Read Offset Prefix Command
2. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 20h // LP Page IWL Read

Upper Page IWL Read Sequence

1. 2Eh: [Offset1(rL2_3bpc), Offset2 (rL4_3bpc), Offset3 (rL6_3bpc)] // Read Offset Prefix Command
2. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 20h // UP IWL Read

eXtra Page IWL Read Sequence

1. 2Eh: [Offset1(rL3_3bpc),Offset2 (rL7_3bpc), Offset3 (00h)] // Read Offset Prefix Command
2. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 20h // XP IWL Read

The sequence for doing a MLC Shared Page IWL Read or a SLC Edge IWL Read would follow similar flow as the MLC Shared Page Read and SLC Edge Page Read described in the Page Read example sequences with replacement of the 30h command with 20h on IWL Read.

Read Offset Prefix Restrictions

When issuing the READ OFFSET PREFIX (2Eh) Command, the host shall input three address cycles (Read offsets) during the valid operations. Having more than or less that three address cycles is considered invalid.

Host shall issue the READ OFFSET PREFIX (2Eh) Command only prior to a valid array read operation. The host shall not issue the READ OFFSET PREFIX (2Eh) Command before non-Read operations (Ex: Program, Erase commands). A Status Read command between READ OFFSET PREFIX (2Eh) Command and next read operation [2Eh + 3 Address cycles + Status Read (70h/71h/78h/79h) + Valid Read Operation] is not allowed, and the Host will need to reissue the Prefix Offset sequence again. The READ OFFSET PREFIX (2Eh) Command must always be followed by a valid read operation only. Only exception would be the RESET commands (FAh/ FFh/FDh), which are allowed to be issued after the prefix command.

When IWL Read is used, the offsets are specific to the plane group. It is the host's responsibility to track the offset values when using IWL Read.

The legal range of the offsets that the host can issue is -1280mV to +1270mV in 10mV increments. When used in combination with other valid read features, the host is responsible to configure the features such that total read offset doesn't exceed the valid range.

The Read Offsets applied would be persistent and every subsequent read operation would apply the same read offset values (to the originally issued page type) until it is cleared by the host. To clear the read offset values the host would have to issue the prefix command (2Eh) with all 00h offset values to each page type, issue a HARD RESET (FDh) command, or issue a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) to Feature Address 86h: P1-P4 = 00h which will reset all stored Read Offset Prefix values to 00h. Other RESET commands will not clear the read offset values.

Interaction with READ PAGE CACHE SEQUENTIAL (31h)

Read Prefix Offsets are not used or stored when a READ PAGE CACHE SEQUENTIAL (31h) command is issued to the last block, last page of a NAND plane as the page address is not re-read.

Interaction with Read Assist Features

When READ OFFSET PREFIX (2Eh) Command is applied and a Read Retry profile is invoked via the Virtual Address Cycle, then the final offset applied to the read operation would be additive. When Auto Read Calibration Persistence is enabled FA 96h P1[1:0]= 10b, the persistence offsets are also applied to the read. All read offsets would be additive and it is the users responsibility to properly manage them.

When Auto Read Calibration (FA:96h) is enabled the ARC is executed with the read offset applied to it. When Auto Read Calibration (FA:96h) persistence bit is enabled, the subsequent read operation is executed with the read offset and the persistence offset applied to it.

Reset Interaction

All READ OFFSET PREFIX (2Eh) Commands must be followed by a valid read operation. Only RESET commands (FAh, FFh, FDh) are allowed after the 2Eh prefix opcode. If a reset command follows the READ OFFSET PREFIX (2Eh) Command or if RESET (FFh) is given before the read algo completes the transfer of prefix data, the offsets are not transferred to Feature Address A0h-ABh Subfeature P1 and P2, and the Host will need to reissue a new 2Eh command for the next read operation.

Reading out Read Offsets

The read offsets issued via the READ OFFSET PREFIX (2Eh) Command can be read out by the host from FA A0h-ABh, Subfeature parameter P1 and P2. FA A0h-ABh are GET only registers.

See Feature Address A0h-ABh Settings Section of the Datasheet for more information on Feature Address assignments and offset readout resolution.

Clearing Read Offsets

To clear the read offset values the host would have to issue the prefix command (2Eh) with all 00h offset values to each page type, issue a HARD RESET (FDh) command, or issue a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) to Feature Address 86h: P1-P4 = 00h which will reset all stored Read Offset Prefix values to 00h. Other RESET commands will not clear the read offset values.

Example Sequence for Clearing Read Offsets

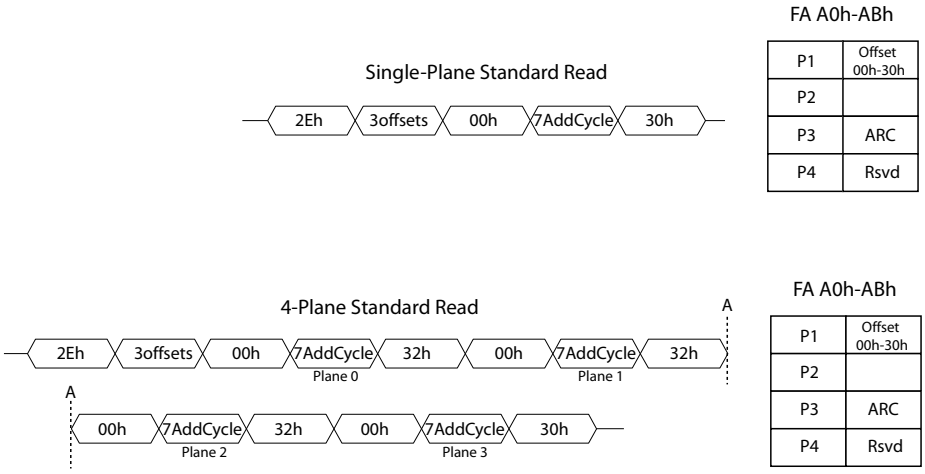
TLC Lower Page Read Sequence

1. 2Eh: [Offset1(rL1_3bpc), Offset2 (rL5_3bpc), Offset3 (00h)] // Read Offset Prefix Command
2. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 30h // LP Page Read with applied read offsets
3. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 30h // LP Page Read with applied read offsets **PERSISTENT**
4. 2Eh: [Offset1(00h), Offset2 (00h), Offset3 (00h)] // Read Offset Prefix Command with 00h applied to all 3 Offsets
5. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 30h //Default LP Page Read with no applied read offsets, **Offsets are cleared**

READ PAGE (00h-30h) and IWL READ (00h-20h) Offset Location

When a READ OFFSET PREFIX (2Eh) Command is issued before a READ PAGE (00h-30h) operation, only Subfeature parameter P1 of FA A0h-ABh is populated. This is the case for both single plane and multi-plane read operations, only Subfeature parameter P1 is populated.

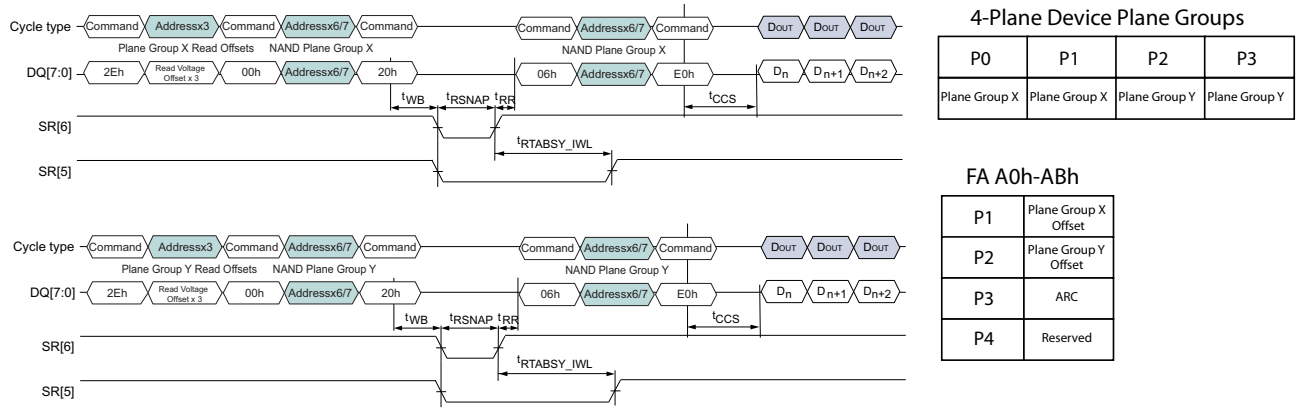
Figure 80: Standard Read - Single and Multiplane Offset Location



Note: 1. 7AddCycle will be used when ACRR is enabled. 6AddCycle will be used when ACRR is not enabled.

When a READ OFFSET PREFIX (2Eh) Command is issued before an IWL READ (00-20h) operation, and if the IWL Read is issued to a page on Plane Group X, then Subfeature parameter P1 is populated, and if the IWL Read is issued to a page on Plane Group Y, then Subfeature parameter P2 is populated

Figure 81: IWL Read IWLx2 Offset Location



Note: 1. 7AddCycle will be used when ACRR is enabled. 6AddCycle will be used when ACRR is not enabled.

The values populated in Subfeature parameter P2 are only used when an IWL Read operation is performed on Plane Group Y.

Multi-Plane Operation

During Multi-plane read operation, the user shall issue 2Eh once at the beginning of the multi-plane sequence and the NAND will use it for reads on all the active planes. It is an atomic sequence and it is not allowed to issue other 2Eh to break this sequence. On sequential cache read, NAND shall use the offset from previous read sequence. During Cache read, it is user's responsibility to track the read offset

issued when cache read crosses the block boundary. If not changed by user, NAND will use the same read offset values across the blocks. See detail in Multi-Plane Read Operation Applied Prefix Offset table.

Table 58: Multi-Plane Read Operation Applied Prefix Offset

2Eh Command	1st Plane Read	2nd Plane Read	3rd Plane Read	4th Plane Read	Offset Applied to Plane(s)
2Eh-Offset	00h-Plane0-32h	00h-Plane1-32h	00h-Plane2-32h	00h-Plane3-30h	Offset applied to Plane 0-3
2Eh-Offset	00h-Plane3-32h	00h-Plane2-32h	00h-Plane1-32h	00h-Plane0-30h	Offset applied to Plane 0-3
2Eh-Offset	00h-Plane1-32h	00h-Plane2-30h			Offset applied to Plane 1-2
no offset	00h-Plane0-32h	00h-Plane1-32h	00h-Plane2-32h	00h-Plane3-30h	Previous Offset (if not cleared by the host) applied to Plane 0-3 for that page type
no offset	00h-Plane3-32h	00h-Plane2-32h	00h-Plane1-32h	00h-Plane0-30h	Previous Offset (if not cleared by the host) applied to Plane 0-3 for that page type
no offset	00h-Plane3-32h	00h-Plane2-30h			Previous Offset (if not cleared by the host) applied to Plane 2-3 for that page type

Table 59: Valid Commands and Feature Addresses

2Eh Command Operation	Result
READ OFFSET PREFIX (2Eh) Command + Read Series Operation (00h-30h, 00h-35h)	Valid
READ OFFSET PREFIX (2Eh) Command+ Read Page Multi Plane (00h-32h)	Valid
READ OFFSET PREFIX (2Eh) Command + Read Page Cache Sequential (31h)	Valid
READ OFFSET PREFIX (2Eh) Command + Read Page Cache Random (00h-31h)	Valid
READ OFFSET PREFIX (2Eh) Command + Read Page Cache Last (3Fh)	Ignored
READ OFFSET PREFIX (2Eh) Command + IWL READ (00h-20h)	Valid [1]
READ OFFSET PREFIX (2Eh) Command + SBSBR (00h-34h)	Valid
READ OFFSET PREFIX (2Eh) Command + Multi-Plane SBSBR (00h-32h)/(00h-34h)	Valid
SLC OTF: 3Bh+READ OFFSET PREFIX (2Eh) Command+Valid Read command (listed above)	Valid
AUTO READ CALIBRATION (FA:96h)	Valid
Address Cycle Read Retry (ACRR)	Valid

Notes: 1. Independent Read Offsets can be applied to each Plane Group

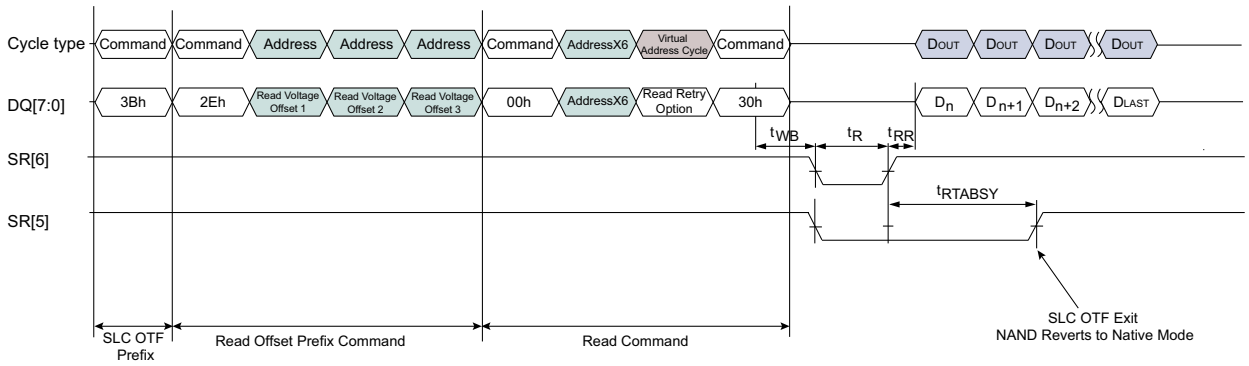
Using READ OFFSET PREFIX (2Eh) Command with SLC OTF Command (3Bh)

When the host wants to apply a read offset to a SLC page using SLC OTF method the following sequence needs to be used.

SLC OTF Page Read example sequence

1. SLC MODE LUN ENABLE (3Bh)
2. 2Eh: [Offset1(rSLC), Offset2 (00h), Offset3 (00h)] // Read Offset Prefix Command
3. 00h: [6 Address Cycles, Virtual Address Cycle (when enabled)], 30h // SLC Page Read with applied read offsets
4. After Read is executed, the part reverts to TLC state.

Figure 82: READ OFFSET PREFIX (2Eh) Command during SLC OTF with ACRR Enabled



IWL READ (00h-20h)

IWL READ (Independent Word Line Read) command provides the fastest possible read of a fully programmed page. This command is accepted by the plane when it is ready (RDY=1, ARDY = 1 or 0). IWL READ (00h-20h) is a SNAP READ with additional restrictions due to the independent plane group operation. IWL Read can be enabled via Opcode 00h-6add-20h or Opcode 00h-7add-20h with ACRR Enabled. IWL READ (00h-20h) must be followed by a CHANGE READ COLUMN ENHANCED (06h-E0h) or a CHANGE READ COLUMN ENHANCED (00h-05h-E0h) command to enable data output.

Figure 83: IWL READ (00h-20h) Operation

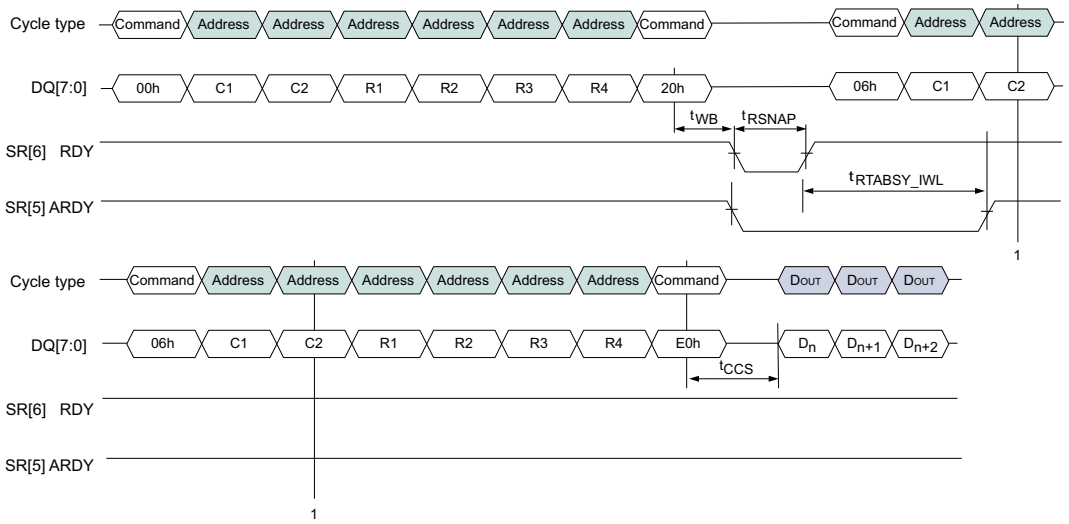
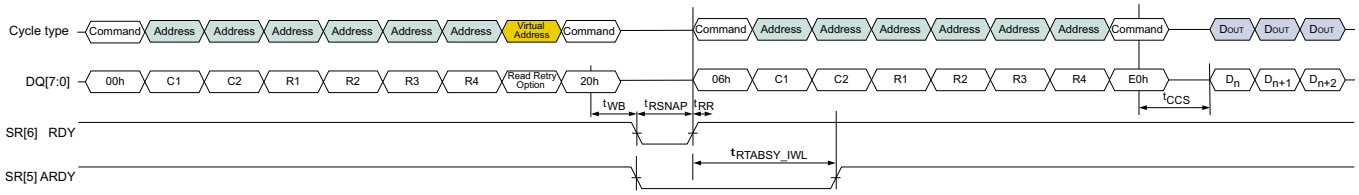


Figure 84: IWL READ (00h-20h) Operation with ACRR Enabled



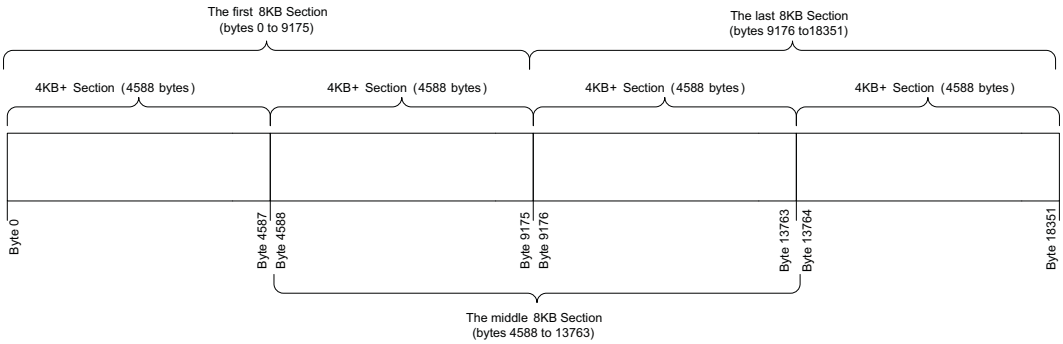
IWL Read Feature

The IWL READ command allows for a fixed 8KB+ section of a page to be read, providing fastest possible ^{t}R times.

When the IWL READ is issued, the read operation will occur within a fixed 8KB+ section of a page. Only data within the enabled 8KB+ section will be available for data output. If the column byte address specified by the IWL READ is part of the second 4KB+ section of the page (bytes 4588 - 9175), then the read operation will enable both 8KB+ fixed logical sections, but only bytes in columns 4588 -13,763 will be readable due to still only enabling the bytes in this section of the page. The page has 3 fixed 8KB+ logical sections: bytes 0 - 9175, bytes 4588 - 13,763, and bytes 9176 - 18,351 (each section contains 2 x 4KB+ sections). When the IWL READ is issued, the byte address specified by the command will determine which section of the page to be read. It is not necessary to address the first byte in a particular section during a read operation. Addressing any byte within the first 4KB+ section (bytes 0 - 4587) will activate the first 8KB+ section (bytes 0 - 9175); Addressing any byte within the second 4KB+ section (bytes 4588 - 9175) will activate the middle 8KB+ section (bytes 4588 - 13,763); Addressing any byte within the third or fourth 4KB+ sections (bytes 9176 - 13,763 or bytes 13,764 - 18,351) will activate the last 8KB+ section

(bytes 9176 - bytes 18,351). CA0 is forced to 0 internally, so start byte address is always an even byte. Data will be invalid for byte addresses not included in the selected 8KB+ section(s) of the page.

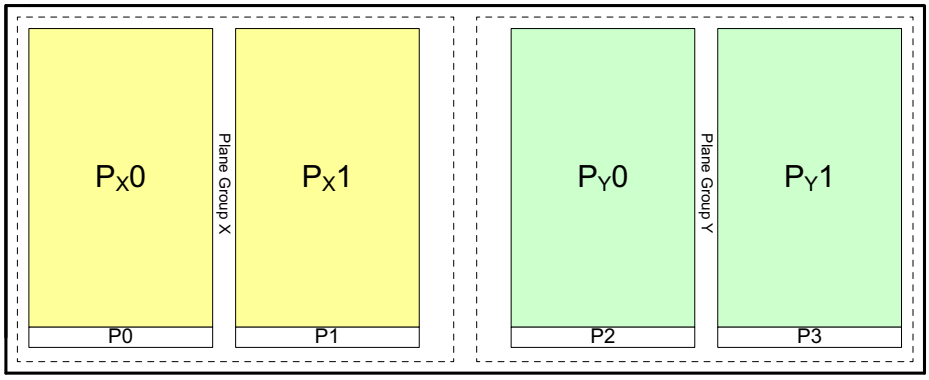
Figure 85: Example of Fixed 8KB+ Length Sections



Independent Word Line Operation

Independent Word Line (IWL) is intended to allow additional parallelism when reading from a single die. The die is divided into two plane groups, each plane group has 2 planes. The additional parallelism is accomplished by enabling the die to accept read commands on a different plane group, while the current plane group is busy with its own read operation. This allows for 'multi-LUN' like operations, within a single LUN, improving read concurrency.

Figure 86: Plane Group Diagram



This capability shall only be used with IWL READ (00h-20h).

Command Concept

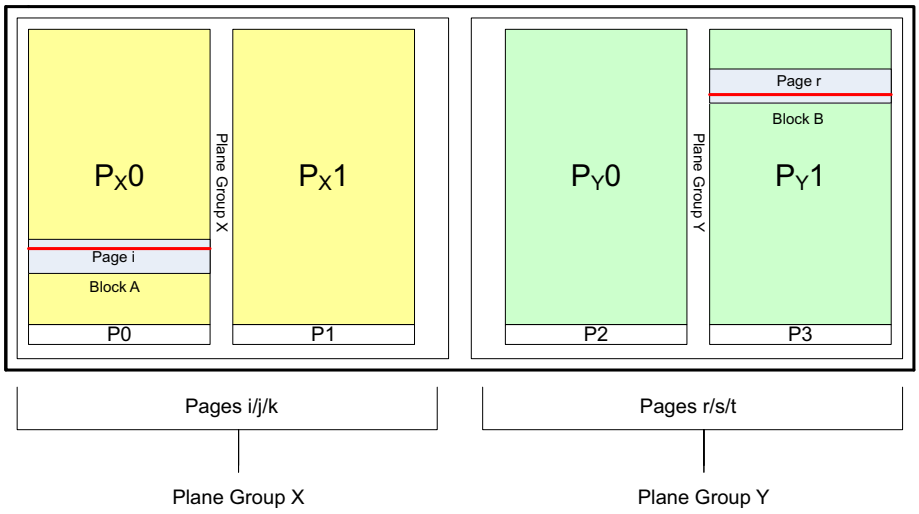
IWL READ will enable read commands to be entered on a different plane group, while the current plane is busy. IWLx2 utilized by the device will utilize plane groupings and allow the Host to conduct IWL READ on each plane group.

This feature will require there to be unique status register bit SR[6] and SR[5] by plane group for the HOST to query. The die SR[6] will be an AND of the SR[6] values of all plane groups. The die ARDY will be an AND of the SR[5] values of all plane groups. For the HOST to determine a unique SR[6] or SR[5] plane group value, the use of the 78h (Read Status Enhanced) command to address the required plane group's status register will be necessary. The 70h (Read Status) and 71h (Fixed Address Read Status Enhanced) will result in a busy if either of the plane groups are busy.

Issuing an IWL READ command to an adjacent plane group while the current plane is busy is allowed and the page number issued to the adjacent plane group can be unique. Issuing read commands

within the same plane group is not allowed in IWL READ. Issuing read commands within the same plane group is allowed with legacy reads (non-IWL READ), however the page address needs to be the same within each plane group. The example below represents the device with IWLx2.

Figure 87: IWLx2 Control on 4 plane device



IWL Restrictions

Status Register

- SR[0] and SR[1] do not shift during IWL READ and should be considered invalid once IWL READs are issued.
- SR[4] is a don't care during IWL READ.
- IWL READ has unique status register bits SR[6] and SR[5] for the host to query. The READ STATUS ENHANCED (78h) command will always return the Plane Group Status Register instead of the Global Status Register. In order to know the overall ready/busy status of the LUN, the user must issue a READ STATUS (70h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command, or issue a READ STATUS ENHANCED (78h) command on each Plane Group and combine the output. Please reference Status Operations section for status behavior for IWL READ.
- Due to the asynchronous nature of IWL READ, there is a possibility of SR[4] being updated and reset before the HOST is able to read its content. SR[4] should be handled as a don't care but in the case it is caught, the system can proceed with its normal Enhanced Status Register check protocol.

Read Offset/Read Offset Prefix

- Read Offset for IWL READ operation is not valid for non-IWL READ operation and Read Offset for non-IWL READ operation is not valid for IWL READ operation. User is required to issue offset 00h to reset the Read Offset value.
- READ OFFSET PREFIX (2Eh) will be supported with IWL READ.
- The Read Offset applied would be persistent per plane group and every subsequent read operation would apply the same read offset values (to the originally issued page type) until it is cleared by the host. To clear the read offset values the host would have to issue the READ OFFSET PREFIX (2Eh) Command with all 00h offset values to Subfeature P1 and P2, or a HARD RESET (FDh). FEATURE ADDRESS A0h-ABh Subfeatures P1/P2 are read only with GET FEATURE (EEh), the values will only be set when using READ OFFSET PREFIX (2Eh) Command. Issuing a SET FEATURE (EFh) command is considered an invalid operation.

- When a READ OFFSET PREFIX (2Eh) Command is issued before an IWL READ (00-20h) operation, and if the IWL READ is issued to a page on Plane Group X, then FEATURE ADDRESS A0h-ABh Subfeature parameter P1 is populated. If the IWL READ is issued to a page on Plane Group Y, then FEATURE ADDRESS A0h-ABh Subfeature parameter P2 is populated.

Read Assist Feature Interaction

- IWL READ is supported with the following read assist features: Read Offsets applied via the READ OFFSET PREFIX (2Eh) Command and Address Cycle Read Retry offsets.
- IWL READ has restrictions and will not perform read features even if they are enabled. If IWL READ is issued when FEATURE ADDRESS (96h): Auto Read Calibration is enabled, IWL READ will be executed regardless, but the ARC persistent offsets will not be applied.

SLC Mode

- This device supports 3Bh: SLC mode entry command with auto exit. A 3Bh command proceeding an IWL READ command will read the addressed plane in SLC mode and revert to TLC mode upon completion of the IWL READ operation. In IWL, a SLC or TLC IWL READ to PlaneGroupX will be independent of PlaneGroupY SLC or TLC IWL READ operation. If the 3Bh command is followed by an invalid sequence or an algo interruption, the device will revert to TLC mode.
- IWL READ will be supported for mixed SLC/TLC operations between different plane groups. (When used with prefix offset, 3Bh is issued before 2Eh). IWL READ SLC/TLC mixed mode operations will be supported during suspend.

Other

- IWL can only be used with IWL READ (00-20h) commands. All other execution commands, including other read commands, are not allowed.
- All other commands are illegal until all on-going IWL READs complete and SR[5] for all planes show ready status (SR[5] = 1).
- If there are no on-going IWL READs, IWL READ cannot be issued until all planes show SR[5]=1. This signifies all non-IWL READ commands have completed and IWL READs are now legal inputs.
- RESET (FFh, FAh) operations will reset the entire LUN and not just the addressed Plane Group.
- IWL READ (00h-20h) must be followed by a CHANGE READ COLUMN ENHANCED (06h-E0h) or a CHANGE READ COLUMN ENHANCED (00h-05h-E0h) command to enable data output.
- IWL READ command (00h-20h) shall not be used as part of COPYBACK PROGRAM (85h-10h) operation.
- If a 00h command is issued to a LUN followed by address cycle input and no valid subsequent confirm command for that operation is issued (i.e. 05h, 20h, 30h, 31h, 32h, 34h, 35h, etc), a RESET (FFh, FAh) command is required before another 00h command can be issued to that LUN to start a new read operation sequence, or to start that LUN's read operation over without executing that operation (i.e. repeating or changing Address Cycle input again).
- The host shall not issue any SET FEATURE (EFh), SET FEATURE BY LUN (D5h), GET FEATURE (EEh), or GET FEATURE by LUN (D4h) operation when an IWL READ (00h-20h) is ongoing. The user needs to wait until all read threads are completed before issuing these operations.
- IWL READs can be issued during program data interruptions. IWL can be issued on any plane, not just the current program plane.

Table 60: List of Valid NAND Array Operations Interaction with IWL

Operation	IWL Support
PROGRAM (80h-10h, 80h-11h, 80h-15h) Operations	No
ERASE (60h-D0h, 60h-D1h) Operations	No

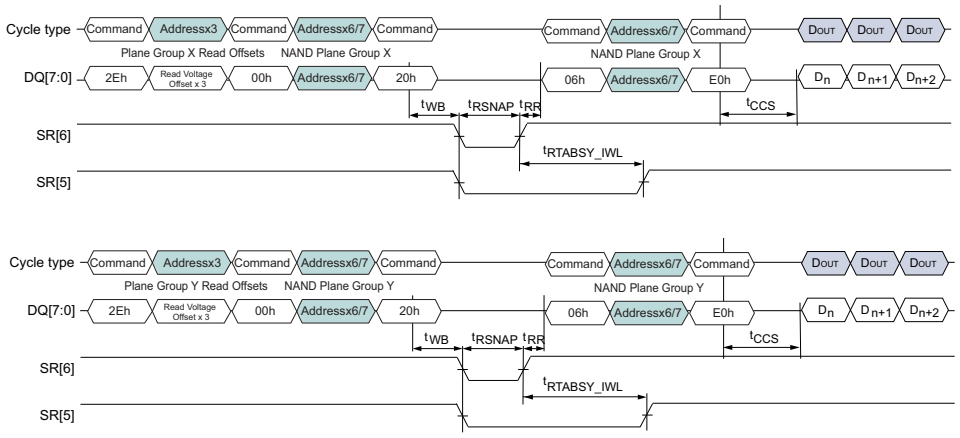
Table 60: List of Valid NAND Array Operations Interaction with IWL (Continued)

Operation	IWL Support
PROGRAM SUSPEND (84h) (In suspended state)	Yes
ERASE SUSPEND (61h) (In suspended state)	Yes
READ PAGE (00h-30h)	No
READ CACHE Series (00h-31h, 31h, 3Fh)	No
READ MULTI-PLANE (00h-32h)	No
COPYBACK READ (00h-35h)	No
SBSBR (00h-34h)	No
OTP Program	No
OTP Read	No
Read Unique ID / Read Param Page	No
READ STATUS (78h-ADDR, 71h-ADDR, 79h-ADDR)	Yes
CHANGE READ COLUMN ENHANCED (06h-E0h or 00h-05h-E0h)	Yes

Table 61: Read Feature Compatibility Table

Feature	Supported?	Different Offset Values Allowed on Different Plane Groups?
Auto Read Calibration (ARC)	No	No
SBSBR	No	No
ACRR	Yes	Yes
Read Offset Prefix - with persistence	Yes	Yes
ARC persistence	No	No

Figure 88: FEATURE ADDRESS A0h-ABh Offsets for 2 Plane Group IWL



4-Plane Device Plane Groups

P0	P1	P2	P3
Plane Group X	Plane Group X	Plane Group Y	Plane Group Y

FA A0h-ABh

P1	Plane Group X Offset
P2	Plane Group Y Offset
P3	ARC
P4	Reserved

Figure 89: IWLx2 Timing Sequence for 00h-20h (1 of 2)

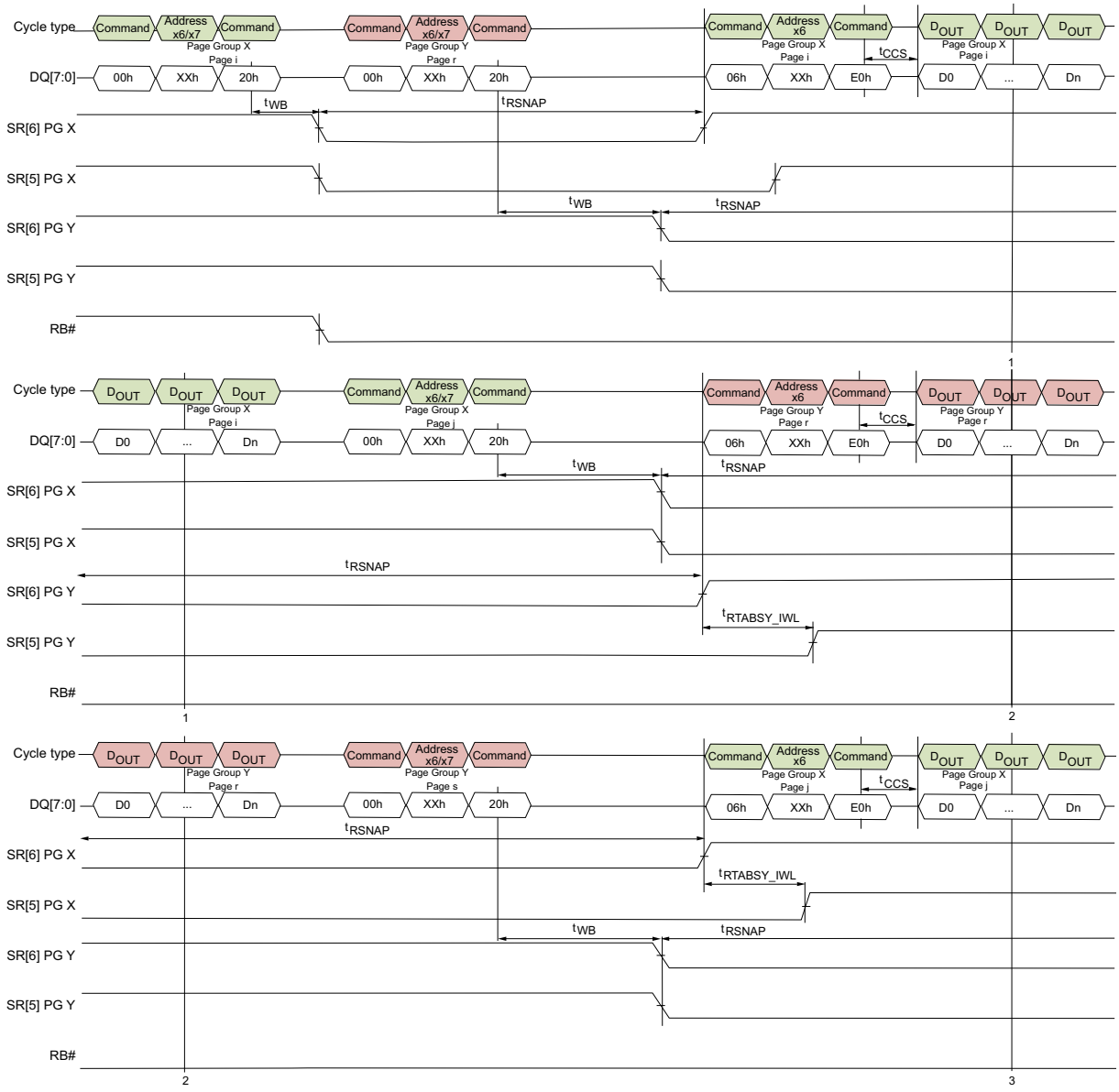
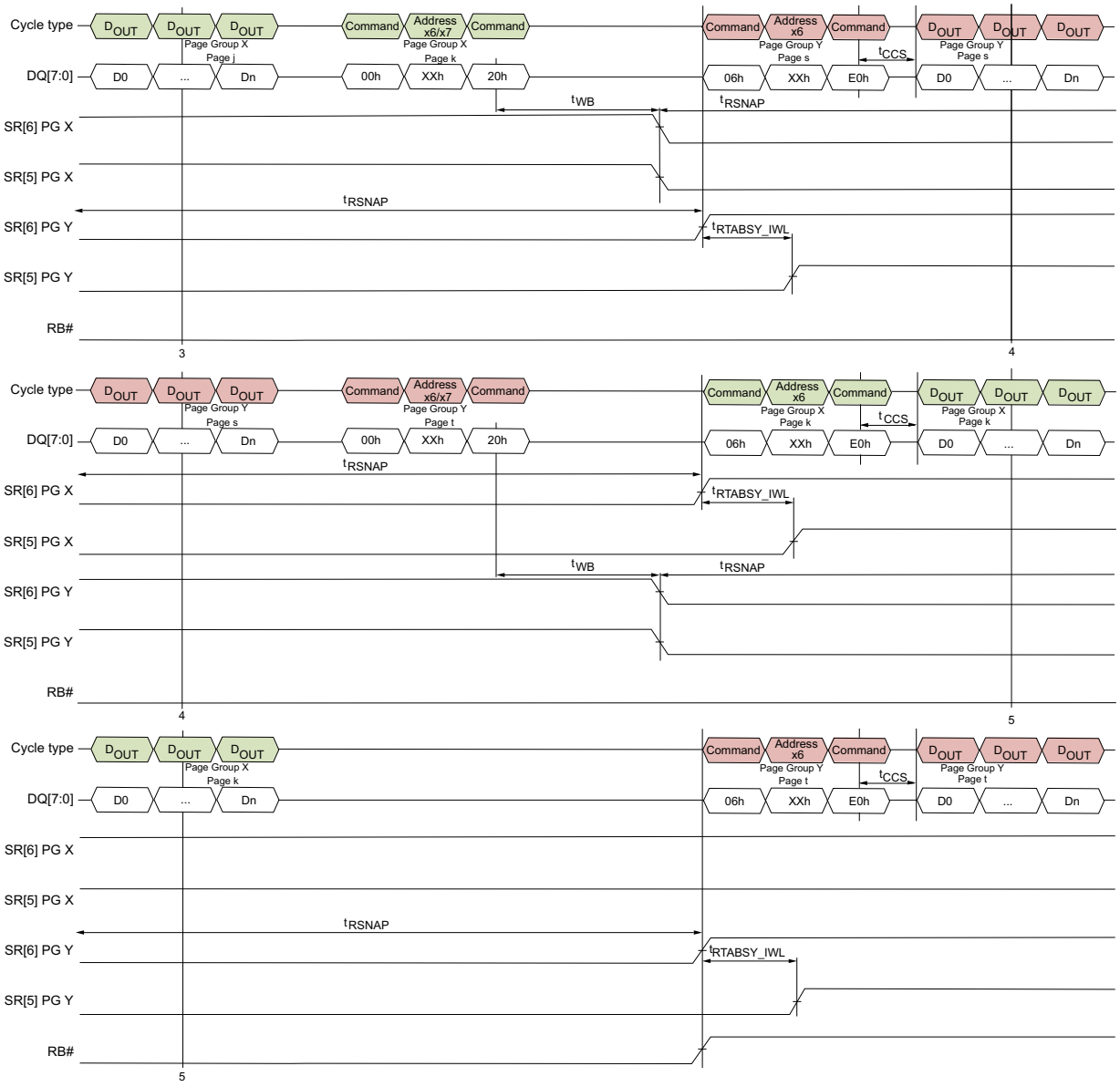


Figure 90: IWLx2 Timing Sequence for 00h-20h (2 of 2)



FEATURE ADDRESS A0h-ABh

FEATURE ADDRESS A0h-ABh store read offset settings from READ OFFSET PREFIX (2Eh) command and Auto Read Calibration (Feature Address 96h). The NAND device will reload the default settings (00h) to FEATURE ADDRESS A0h-ABh Subfeature P1, P2, P3 after the host issued HARD RESET (FDh) command. Issuing a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) to Feature Address 86h: P1-P4 = 00h will clear all previous stored Read Offset Prefix values stored in Feature Address A0h-ABh Subfeature P1 and P2 to 00h. Other than read offsets issued via the READ OFFSET PREFIX (2Eh) Command, no other commands will change the settings of FEATURE ADDRESS A0h-ABh Subfeature P1 and P2. FEATURE ADDRESS A0h-ABh Subfeature P3 will be set by Auto Read Calibration.

The read offsets issued via the READ OFFSET PREFIX (2Eh) Command can be read out by the host from FA A0h-ABh, Subfeature parameter P1 and P2. The calibrated offset values calculated using FEATURE ADDRESS 96h (Auto Read Calibration) can be read out by the host from FA A0h-ABh, Subfeature parameter P3. FA A0h-ABh are get only features.

Final Read level is defined as:

- Persistence ON:*default read level + FEATURE ADDRESS A0h-ABh offset value (SubFeature P1 or P2) + Address Cycle Read Retry offset (if enabled) + SBSBR offset (if enabled) + calibrated offset value (FEATURE ADDRESS A0h-ABh SubFeature P3)*
- Persistence OFF: *default read level + FEATURE ADDRESS A0h-ABh offset value (SubFeature P1 or P2) + Address Cycle Read Retry offset (if enabled) + SBSBR offset (if enabled)*

The Feature Addresses allocated for the read verify levels are listed in Definitions for Feature Addresses A0h-ABh Table with an internal circuit resolution of 10mV.

Table 62: FEATURE ADDRESS A0h-ABh Settings

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
READ PAGE (00h-30h)/IWL Read Offset Plane Group X	Read Only	X	X	X	X	X	X	X	X	rSLC, rSLC_edge, r[1-3]_2bpc, r[1-7]_3bpc	1,2
P2											
IWL Read Offset Plane Group Y	Read Only	X	X	X	X	X	X	X	X	rSLC, rSLC_edge, r[1-3]_2bpc, r[1-7]_3bpc	1,2
P3											
Calibrated Read Offset Value	Read Only	X	X	X	X	X	X	X	X	rSLC, rSLC_edge, r[1-3]_2bpc, r[1-7]_3bpc	3
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. See Definitions for Feature Addresses A0h-ABh table for read level references.
2. See FEATURE ADDRESS A0h-ABh: P1/P2/P3 Sub-feature Values and Corresponding Offset Voltage Values table to determine P1 and P2 value for a given voltage offset value.
3. The calibrated offset values from Auto Read Calibration operations are stored in the P3 Sub-features. See Reading out Calibrated offsets in the Auto Read Calibration sub-section for details.

Table 63: Definitions for Feature Addresses A0h-ABh

Feature Address	WL Type	Page Type	Applied Read Offset Level	Description
A0h	MLC	Upper Page	rL1_2bpc	L1 Read Offset for fully programmed MLC Shared Page (2bpc)
A1h	MLC	Lower Page	rL2_2bpc	L2 Read Offset for fully programmed MLC Shared Page (2bpc)
A2h	MLC	Upper Page	rL3_2bpc	L3 Read Offset for fully programmed MLC Shared Page (2bpc)
A3h	-	-	-	Reserved
A4h	SLC	SLC Page	rSLC/rSLC_Edge	SLC Read Offset level for SLC programmed SLC Page (1bpc)
A5h	TLC	Lower Page	rL1_3bpc	L1 Read Offset for fully programmed TLC Shared Page (3bpc)
A6h	TLC	Upper Page	rL2_3bpc	L2 Read Offset for fully programmed TLC Shared Page (3bpc)
A7h	TLC	eXtra Page	rL3_3bpc	L3 Read Offset for fully programmed TLC Shared Page (3bpc)
A8h	TLC	Upper Page	rL4_3bpc	L4 Read Offset for fully programmed TLC Shared Page (3bpc)
A9h	TLC	Lower Page	rL5_3bpc	L5 Read Offset for fully programmed TLC Shared Page (3bpc)
AAh	TLC	Upper Page	rL6_3bpc	L6 Read Offset for fully programmed TLC Shared Page (3bpc)
ABh	TLC	eXtra Page	rL7_3bpc	L7 Read Offset for fully programmed TLC Shared Page (3bpc)

Notes: 1. MLC refers to only 2 shared pages; TLC refers to 3 shared pages. Refer to the Shared Pages section for details.

Figure 91: Read Offset Levels for Feature Addresses A0h-ABh

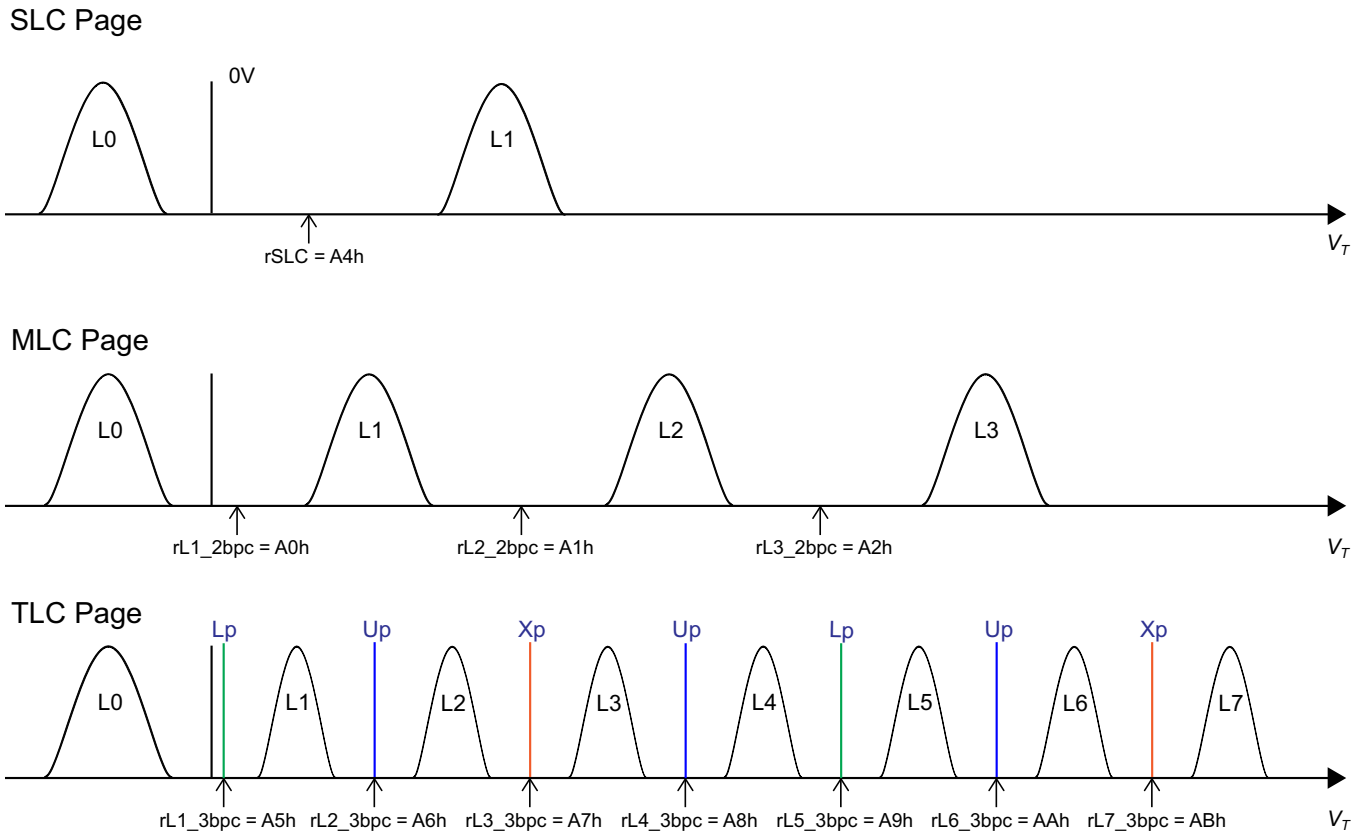


Table 64: FEATURE ADDRESS A0h-ABh: P1/P2/P3 Sub-feature Values and Corresponding Voltage Offset Values

P1/P2/P3 Sub-feature Value	Voltage Offset Value
00h	0V
01h	10mV
02h	20mV
03h	30mV
04h	40mV
05h	50mV
.	.
.	.
7Ch	1240mV
7Dh	1250mV
7Eh	1260mV
7Fh	1270mV
80h	-1280mV
81h	-1270mV
82h	-1260mV

Table 64: FEATURE ADDRESS A0h-ABh: P1/P2/P3 Sub-feature Values and Corresponding Voltage Offset Values (Continued)

P1/P2/P3 Sub-feature Value	Voltage Offset Value
83h	-1250mV
.	.
.	.
FAh	-60mV
FBh	-50mV
FCh	-40mV
FDh	-30mV
FEh	-20mV
FFh	-10mV

Notes: 1. The lowest scan level of rL1_2bpc/rL1_3bpc/rSLC/rSLC_edge might be limited by circuit limitation. Below 0V is not available.
2. The SLC Read Offset level is applied the same on rSLC and rSLC_edge wordlines (On-the-fly SLC mode and SLC pages on a TLC block).

Auto Read Calibration Operations

Maintaining higher level of data integrity is becoming more challenging as both process node of NAND decreases and as the number of bits stored per memory cell increases. To achieve higher level of data integrity and reliability throughout the lifetime of a NAND device it is becoming more important to properly calibrate read levels to match the condition of the NAND block. The Auto Read Calibration (Feature Address 96h) feature provides an automated algorithm where the NAND device optimizes the read level for the current data distributions in a given NAND page. This calibrated read level can then be stored in a feature address to allow for continued use without the need to perform additional calibration operations.

The Auto Read Calibration (Feature Address 96h) is a required part of the error recovery flow for the NAND device and can be used prior to, interleaved with, or after Address Cycle Read Retry (Feature Address 96h) operations so long as every combination is utilized by the host before declaring a read failure. This flexibility in utilizing the Auto Read Calibration (Feature Address 96h) function permits a host system to best optimize for read latencies for a given use condition of the NAND device and taking advantage of error handling capabilities of a host system.

Auto Read Calibration

The Auto Read Calibration function is used in an attempt to "calibrate" the read level with the current life condition of a block. This is accomplished by analyzing the data threshold distributions of the page being read and then providing a new threshold decision point for the page. The calibrated read level can be used for the subsequent reads to achieve optimal bit error rate performance on wordlines/blocks that share the life cycle and condition of the calibrated wordline. The Auto Read Calibration functionality can be used to optimize Lower Page read levels (rL2_2bpc, rL1_3bpc, and rL5_3bpc), Upper Page read levels (rL1_2bpc, rL3_2bpc, rL2_3bpc, r4L_3bpc, and rL6_3bpc), eXtra Page read levels (rL3_3bpc and rL7_3bpc) as well as SLC Page read levels (rSLC) independently of one another. In the case of SLC wordline or SLC configured block, the calibration will be performed using the rSLC read level.

If Calibration Read is enabled, the read operation will gather data for all thresholds associated with the READ PAGE being performed and calibrate the read levels for that page. The NAND device will then

perform another read on the same page with the calibrated offset, and the data available to be transferred out of the device will reflect the calibrated read levels. When Calibration Read is enabled, the calibration algorithm will start with the current default read level plus any applied offsets (such as Read Offset Prefix or Address Cycle Read Retry offset).

Using the Persistence bit, the Auto Read Calibration feature offers the capability to store the calibrated offset values which can be used for subsequent pages reads. If Persistence is enabled, the calibrated offset is additive with any other offsets applied such as Read Offset Prefix or Address Cycle Read Retry (Feature Address 96h).

If Auto Read Calibration (Feature Address 96h) subfeature P1 DQ[1:0] = 01b - Calibration enabled with Persistence OFF is set, the issued read will run calibration by gathering data for all thresholds associated with the READ PAGE being performed, store the calibrated offset and then perform another read on the same page with the calibrated read level. Calibration enabled will only calibrate the read levels for the page type being read. For example, if a lower page read is issued on a fully programmed TLC wordline, rL1_3bpc and rL5_3bpc read levels will be calibrated, and then after calibration the calibrated values will be used for the read. If a upper page read is issued on a fully programmed TLC wordline, rL2_3bpc, rL4_3bpc, and rL6_3bpc levels will be calibrated, after calibration the calibrated values will be used for the read.

If Auto Read Calibration (Feature Address 96h) subfeature P1 DQ[1:0] = 10b, Calibration disabled with Persistence ON is set, the issued read will not run calibration, but will use the previously stored calibration offset values for the read. This functionality is useful if the page being read is expected to have similar distributions, that is, it shares the same or similar life cycle and condition as the page where the previous calibration was performed. The Calibration offset values will be stored and accessible via GET FEATURE for Feature Addresses A0h-ABh, sub-feature parameter P3 until they are overwritten with the next calibration. Any subsequent Program, Read or Erase operation with Persistence OFF will not clear the stored calibration offset values.

If Auto Read Calibration (Feature Address 96h) subfeature P1 DQ[1:0] = 00b - Calibration disabled and Persistence OFF is the default setting in which the issued read will use default read levels and all previously calibrated offsets will not be added to the read levels, but the offset values will not be cleared. A read performed with Persistence off will not clear the calibrated offsets.

If Auto Read Calibration (Feature Address 96h) subfeature P1 DQ[1:0] = 11b - Calibration enabled with Persistence ON is set, the issued read will run calibration starting the calibration at the previously calibrated offsets, store the new calibrated values, and will use the new calibration offset values for the read. The Calibration offset values will be stored until they are overwritten with the next calibration. Persistence ON allows continued use of the calibrated values on subsequent reads and calibrations. If the optimal read location is located outside of calibration search, repeated calibrations may be required to find the optimal read location.

Table 65: Behavioral Summary for Auto Read Calibration Feature

FA 96h P1 DQ[1:0]	Persistence	Calibration
00b	OFF - All previously stored calibrated offsets will not be added to the read levels, and the offset values will not be cleared	OFF - Read will use default read levels and calibration will not be performed
01b	OFF - All previously stored calibrated offsets will not be added to the read levels during calibration, and only the previously stored calibrated read offsets for the page type being read will be overwritten	ON - Calibration will be performed using default read levels, the optimum offset for each page type being read will be stored in the persist offset location and used during the actual read

Table 65: Behavioral Summary for Auto Read Calibration Feature (Continued)

FA 96h P1 DQ[1:0]	Persistence	Calibration
10b	ON - All previously stored calibrated offsets will be added to the read levels, and the offset values will not be cleared	OFF - Read will use previously stored calibrated offsets and calibration will not be performed
11b	ON - All previously stored calibrated offsets will be added to the read levels during calibration, and only the previously calibrated read offsets for the page type being read will be overwritten	ON - Calibration will be performed using previously stored calibrated offsets, the optimum offset for each page type being read will be stored in the persist offset location and used during the actual read

If READ PAGE MULTI-PLANE (00h-32h) is used while Auto Read Calibration is enabled, the calibration offset values will come from the block associated with the least significant plane address. It is prohibited to use this feature on unbalanced planes. If READ PAGE MULTI-PLANE is used after Auto Read Calibration has been disabled and Persistence enabled, the offset values used for the read will be associated with the block associated with the least significant plane address. If Persistence is enabled PAGE READ CACHE functions will also use the Calibration offset values stored for the previous calibration. If Auto Read Calibration is enabled any PAGE READ CACHE functions are not allowed.

An IWL READ (00h-20h) issued when Auto Read Calibration (96h) is enabled will execute the IWL READ but the ARC persistent offsets will not be applied.

A side effect of Auto Read Calibration functionality is that the calibration extends the NAND array read time to ^{t}RARC for all pages' read while Calibration Read is enabled. After Calibration Read is disabled, normal ^{t}R performance will be observed (even with Persistence enabled).

The RESET (FFh, FAh) commands will not reset the data in the feature address and disable Calibration. A HARD RESET (FDh) command will change all the values of the Calibration feature for the target LUN back to their default values. If RESET occurs during ^{t}RARC, the calibration values are invalid and the calibration is required to be executed again if Persistence mode is used.

These features should not be enabled with the following commands: READ PAGE CACHE (ANY), READ PARAMETER PAGE (ECh), READ UNIQUE ID (EDh), READ OTP PAGE (00h-30h).

Auto Read Calibration and Read Offset Prefix

Auto Read Calibration can be used in conjunction with Read Offset Prefix or Address Cycle Read Retry offset operations to allow for more efficient application of the calibration values. After a Read operation with Auto Read Calibration enabled, the calibration value will be stored in the subfeature parameter P3 of the associated Feature Address (A0h-ABh). The subfeature parameter P3 of this group of Feature Addresses is read only, meaning that the host is unable to perform SET FEATURES (EFh/D5h) operations on the subfeature parameter P3.

It is possible to read the calibration value from the subfeature parameter P3 and apply the value with READ OFFSET PREFIX (2Eh) command and/or Address Cycle Read Retry offset for use during Read operations of pages that are in the same life condition as the calibrated page. The Read Offset Prefix values can be read from subfeature parameter P1 and P2 of the appropriate Feature Address (A0h-ABh) at a later time for use with pages in the same life condition as the calibrated page, preventing the need to re-calibrate each time the page is read. The subfeature parameter P1 and P2 of this group of Feature Addresses is read only, meaning that the host is unable to perform SET FEATURES (EFh/D5h) operations on the subfeature parameter P1 and P2.

If the value read back out of the subfeature parameter P3 is equal to ±90mV (or ±90mV from the previously attained calibrated value), this indicates that the maximum range of Auto Read Calibration function was reached. When the maximum range of Auto Read Calibration is reached it is likely that the

optimal read level was not identified. In this case it is recommended that Auto Read Calibration be run again with the Persistence bit enabled to ensure that the optimal read level is identified. Note in the case of an Lower Page, it is not necessary to run Auto Read Calibration again with Persistence enabled if only the rL1_3bpc (Feature Address A5h) level reaches its maximum range value.

The final applied read voltage will be the sum of the subfeature parameters P1/P2 and P3, the default read level, and any Address Cycle Read Retry option that has been applied. Because of this, care must be taken when using Read Offset Prefix and Auto Calibration Read to ensure that values of the subfeature parameters P1/P2 and P3 are known and applied correctly. If the subfeature parameter P1/P2 contains a value other than 00h and Auto Read Calibration is enabled, the calibration operation will start from the default read level plus the P1/P2 offset value. In this case the calibration value obtained (stored in the subfeature parameter P3) will only be accurate with the same P1/P2 offset value also applied.

It is recommended to reset Read Offset Prefix and Address Cycle Read Retry to a value of 00h prior to enabling Auto Read Calibration. This is because if any Read Offset Prefix or Address Cycle Read Retry is selected and Auto Read Calibration is enabled, the calibration operation will start from the default read level plus the Read Offset Prefix or Address Cycle Read Retry offset value. In this case the calibration value obtained (stored in the subfeature parameter P3) will only be accurate with the same Read Offset Prefix or Address Cycle Read Retry offset value applied. However, for extreme conditions (for example, end of cycling life or long data retention, and so forth.) it might be required to start from a non-default Read Offset Prefix or Address Cycle Read Retry offset value and then run Auto Read Calibration.

In the event that both Read Offset Prefix and Address Cycle Read Retry values are applied at the time Auto Read Calibration is enabled, the calibration operation will start at the default read level plus both Read Offset Prefix and Address Cycle Read Retry offset values and the resulting calibration value will only be valid with both of the same Read Offset Prefix and Address Cycle Read Retry offset values are enabled on the subsequent reads.

Reading out Calibrated offsets with GET FEATURES (EEh/D4h)

The calibrated offset value from Auto Read Calibration operation is stored in the P3 subfeature of Feature Address (A0h-ABh). This stored calibrated offset value can be used for the subsequent pages read, by issuing GET FEATURES (EEh/D4h) command to the feature address. Please see table in Feature Address (A0h-ABh) for voltage offset values.

Address Cycle Read Retry (ACRR) Operations

The Address Cycle Read Retry (Feature Address 96h) is a required part of the error recovery flow for the NAND device and can be used prior to, interleaved with, or after Auto Read Calibration (Feature Address 96h) operations so long as every combination is utilized by the host before declaring a read failure. This flexibility in utilizing the Address Cycle Read Retry (Feature Address 96h) function permits a host system to best optimize for read latencies for a given use condition of the NAND device and taking advantage of error handling capabilities of a host system.

Address Cycle Read Retry operation enables the NAND device to set different read offset levels in order to recover data that is beyond the normal ECC correction threshold. Address Cycle Read Retry must be initialized by the host during device configuration. The Address Cycle Read Retry is implemented by issuing a 7th address cycle during Read operations that contains the offset value. For controllers that cannot implement the offset using Address Cycle Read Retry, the read offset value can be implemented using Read Prefix Offset (2Eh). NAND will support 8 different Read Retry profiles (that is, Profile0 to Profile7). The host shall not issue any profile greater than 07h in the 7th address cycle.

A RESET (FFh/FAh) command will not cause Feature Address 96h: Address Cycle Read Retry to revert to its default values. However, a HARD RESET (FDh) command or a NAND Power Cycle will cause Feature Address 96h: Address Cycle Read Retry to revert to its default value.

Single Bit Soft Bit Read Operations

SINGLE BIT SOFT BIT READ (SBSBR) operations provide one method of retrieving Soft Information or Soft Data from the NAND Flash array. This Soft Data supports the Hard Data to determine the quality of the Hard Data read, or to give more bits of information regarding the relative placement of the data in the cell. When used in conjunction with advanced Error Correction algorithms, it is possible to achieve increased error correction capability.

Using SBSBR operations, it is possible to retrieve any desired number of soft bits. Soft Information bit widths can be configured using SET FEATURE (EFh) or SET FEATURE by LUN (D5h) command to the feature address E1h - E3h and B1h - B4h (The corresponding read level of each feature address in the NAND device referenced in Table: Feature Address E1h-E3h, B1h-B4h: SBSBR Offsets). The positive and negative offset voltages used to create the soft information bin width can be set independently, allowing for asymmetrical soft data bins.

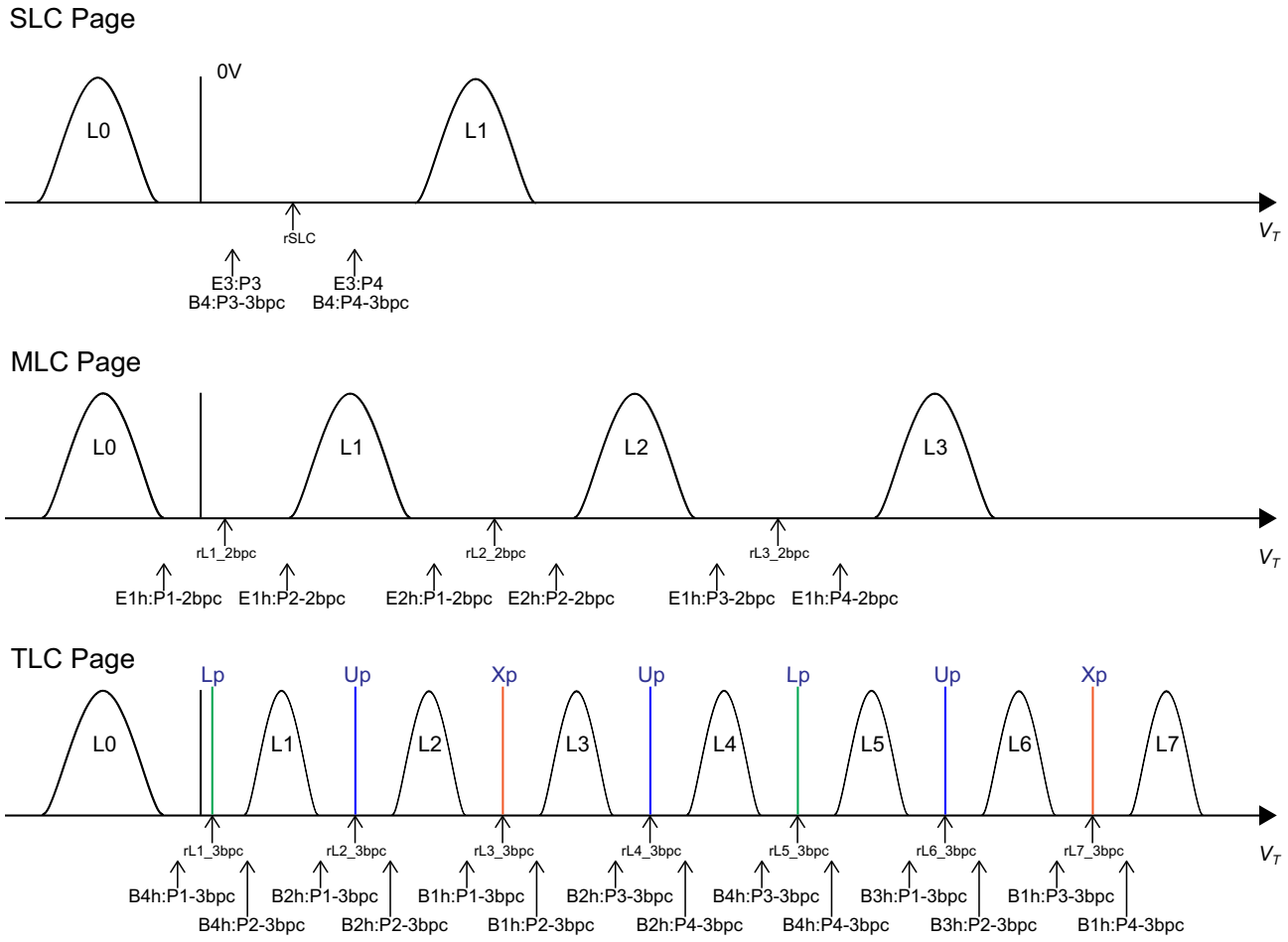
Table 66: Definitions for Feature Addresses B1h-B4h, E1h-E3h

Feature Address	Subfeature Parameter	WL Type	Page Type	Applied Read Level	Description
E1h	P1	MLC	Upper Page	rL1_2bpc	Negative SBSBR Offset for L1 for fully programmed WL
	P2	MLC	Upper Page	rL1_2bpc	Positive SBSBR Offset for L1 for fully programmed WL
	P3	MLC	Upper Page	rL3_2bpc	Negative SBSBR Offset for L3 for fully programmed WL
	P4	MLC	Upper Page	rL3_2bpc	Positive SBSBR Offset for L3 for fully programmed WL
E2h	P1	MLC	Lower Page	rL2_2bpc	Negative SBSBR Offset for L2 for fully programmed WL
	P2	MLC	Lower Page	rL2_2bpc	Positive SBSBR Offset for L2 for fully programmed WL
	P3	–	–	–	Reserved
	P4	–	–	–	Reserved
E3h	P1	–	–	–	Reserved
	P2	–	–	–	Reserved
	P3	SLC	SLC Page	rSLC, rSL-C_edge	Negative SBSBR Offset for SLC only pages
	P4	SLC	SLC Page	rSLC, rSL-C_edge	Positive SBSBR Offset for SLC only pages
B1h	P1	TLC	eXtra Page	r3L_3bpc	Negative SBSBR Offset for L3 for fully programmed WL
	P2	TLC	eXtra Page	r3L_3bpc	Positive SBSBR Offset for L3 for fully programmed WL
	P3	TLC	eXtra Page	r7L_3bpc	Negative SBSBR Offset for L7 for fully programmed WL
	P4	TLC	eXtra Page	r7L_3bpc	Positive SBSBR Offset for L7 for fully programmed WL
B2h	P1	TLC	Upper Page	r2L_3bpc	Negative SBSBR Offset for L2 for fully programmed WL
	P2	TLC	Upper Page	r2L_3bpc	Positive SBSBR Offset for L2 for fully programmed WL
	P3	TLC	Upper Page	r4L_3bpc	Negative SBSBR Offset for L4 for fully programmed WL
	P4	TLC	Upper Page	r4L_3bpc	Positive SBSBR Offset for L4 for fully programmed WL

Table 66: Definitions for Feature Addresses B1h-B4h, E1h-E3h (Continued)

Feature Address	Subfeature Parameter	WL Type	Page Type	Applied Read Level	Description
B3h	P1	TLC	Upper Page	r6L_3bpc	Negative SBSBR Offset for L6 for fully programmed WL
	P2	TLC	Upper Page	r6L_3bpc	Positive SBSBR Offset for L6 for fully programmed WL
	P3	–	–	–	Reserved
	P4	–	–	–	Reserved
B4h	P1	TLC	Lower Page	r1L_3bpc	Negative SBSBR Offset for L1 for fully programmed WL
	P2	TLC	Lower Page	r1L_3bpc	Positive SBSBR Offset for L1 for fully programmed WL
	P3	TLC	Lower Page	r5L_3bpc	Negative SBSBR Offset for L5 for fully programmed WL
	P4	TLC	Lower Page	r5L_3bpc	Positive SBSBR Offset for L5 for fully programmed WL

Figure 92: SBSBR Read Offset Levels for Feature Addresses B1h-B4h, E1h-E3h



The value assigned to each combination of Feature Address (E1h-E3h and B1h-B4h) and subfeature parameters P1-P4 sets the desired SBSBR offset level. It is possible to apply a different value for the negative and positive SBSBR offsets, allowing for asymmetrical soft data bin widths.

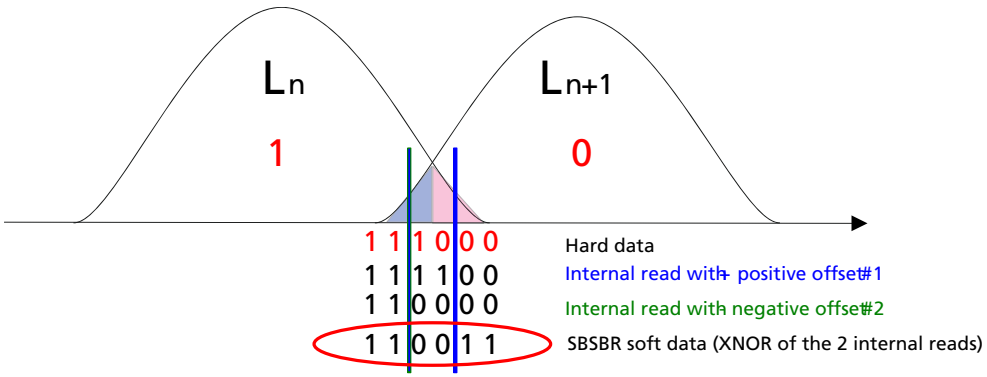
Table 67: SBSBR Subfeature Parameter Setting for Feature Addresses B1h-B4h, E1h-E3h

P1-P4 Subfeature Value	Absolute SBSBR Offset (mV)
00h	0
01h	10
02h	20
03h	30
…	…
…	…
FCh	2520
FDh	2530
FEh	2540
FFh	2550

SINGLE BIT SOFT BIT READ PAGE (00h-34h)

The SINGLE BIT SOFT BIT READ PAGE (00h-34h) command provides a single bit of soft information. Read operations on the NAND Flash array are performed at both the negative and positive offsets for the appropriate read level as defined by Feature Addresses E1h-E3h and B1-B4. The resulting data from the two reads is encoded by an XNOR operation, and then made available for data output. See the figure SBSBR Encoding for illustration. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

Figure 93: SBSBR Encoding



After setting Feature Addresses E1h-E3h and B1h-B4h to the appropriate values, to read a single bit of soft information from a page, issue the 00h command, then issue the required address cycles, and conclude by issuing the 34h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}R_SBSBR as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or status operations (70h, 71h, 78h) can be used. If the status operations are used to monitor the LUN's status, when the die (LUN) is ready (RDY = 1), the host shall disable status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, output begins at the column address specified.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command must be used to select only one die (LUN) prior to issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h / 00h-05h-E0h) to enable data output to prevent bus contention.

The SINGLE BIT SOFT BIT READ PAGE (00h-34h) command can be used as the final command of a multi-plane read operation. It is preceded by one or more READ PAGE MULTI-PLANE (00h-32h) commands. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1), data output is enabled for the cache register linked to the least significant plane addressed, regardless of input order. When the host requests data output, output begins at the column address last specified in the SINGLE BIT SOFT BIT READ PAGE (00h-34h) command. The CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h) command is used to enable data output in the other cache registers.

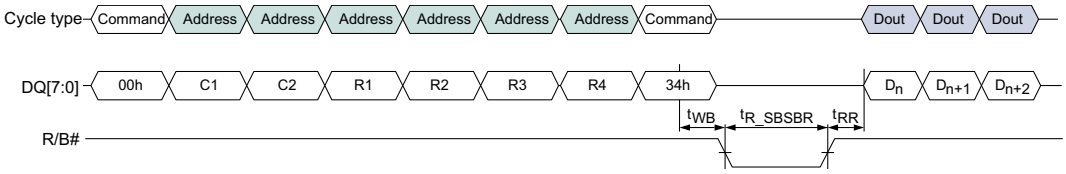
A multi-plane SBSBR operation on "unbalanced" planes (that is, reading the same page type, but all planes addressed do not have the same programmed condition of shared pages) is not allowed. See the Multi-Plane Operations section for additional multi-plane addressing requirements.

During SBSBR operation, Address Cycle Read Retry is supported.

It is not possible to use SBSBR operations in conjunction with IWL READ (00h-20h) operations.

When SBSBR operation is run with Auto Read Calibration enabled (Feature Address 96h P1<0> = 1), no Calibration is performed and only SBSBR sequence is executed. If only Persistence is enabled (Feature Address 96h P1<1> = 1), the stored calibration offsets are incorporated into the SBSBR operation.

Figure 94: SINGLE BIT SOFT BIT READ PAGE (00h-34h) Operation



SLC Operations

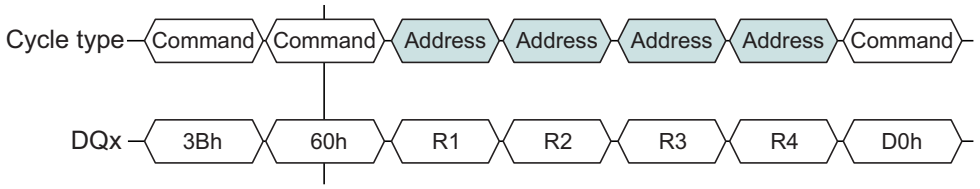
This NAND Flash device supports SLC Operations, within defined limitations. SLC Operations allow the NAND array blocks in this TLC (i.e. 3 bit per cell) device to operate in a SLC (i.e. 1 bit per cell) mode. This device uses SLC MODE LUN ENABLE (3Bh) with Auto Exit. The host will need to ensure that the SLC MODE LUN ENABLE (3Bh) command is entered prior to the desired SLC mode operation and the device will revert to TLC mode when the SLC array operation is complete (ARDY = 1).

Configuration using SLC MODE LUN ENABLE (3Bh) with Auto Exit

SLC Mode operations can be enabled through the use of the SLC MODE LUN ENABLE (3Bh) command. SLC MODE LUN ENABLE (3Bh) command will enable SLC Mode operations on a LUN addressable level.

The addressed LUN used with the SLC MODE LUN ENABLE (3Bh) command will automatically exit SLC Mode upon completion of the SLC array operation (ARDY = 1). For each desired SLC operation, the device will need to have the SLC MODE LUN ENABLE (3Bh) command precede the SLC operation.

Figure 95: SLC MODE LUN ENABLE (3Bh) example with ERASE BLOCK (60h-D0h)



SLC/TLC Mode Operations

When in SLC mode, within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (i.e. 0, 1, 2, 3, …). Programming pages out of order within a block is prohibited.

The device itself does not maintain any tracking of which blocks have been designated as either default mode operational blocks or SLC blocks. Therefore, the host controller must keep track of which blocks have been used in SLC mode. Furthermore, the host must be aware of what mode the device is currently operating in. Micron initializes all blocks with a default mode erase as the last manufacturing step, so the SLC block must be properly "initialized'.

Any block that is being changed from its default mode of operation must be "initialized" with an erase command in the SLC mode. After completion of the erase command, the host can then issue program operations in SLC mode to the previously erased NAND block. To properly "initialize" a block for SLC MODE, the host must first ensure that the block has at least 50% of the pages programmed (either in default mode or in SLC mode) before issuing the first SLC MODE erase. This includes "initialization" if the block is put into the SLC MODE immediately upon first cycle. Micron initializes all blocks with a default mode erase as the last manufacturing step, so the SLC block must be properly "initialized". Any time the device is used in the default mode prior to SLC MODE, the user must ensure that at least 50% of the pages are programmed before the first SLC MODE erase.

Once a NAND block is used in an array operation (PROGRAM/ERASE) in SLC mode, it is not permitted to use that NAND block in the default mode from that point forward. All future array operations on that block must be performed in SLC mode. If a NAND block is used in an array operation (PROGRAM/ERASE) in default mode, it may be changed to be an SLC block if the change occurs within the first 10% of the maximum allowed TLC PROGRAM/ERASE cycles or within 300 TLC PROGRAM/ERASE cycles (whichever is less) of that block's use. It is the responsibility of the host to keep track of how many cycles have occurred.

It is imperative that the device is in the corresponding mode that a given block has been designated as. This applies to all PROGRAM, ERASE, and READ sequences. Mixing pages of different modes within a block is prohibited. For example, programming a page in a block, which was programmed in SLC mode, while in default mode, or vice versa, will result in the data corruption.

The host must ensure that it does not mix TLC and SLC modes during any single operation. For example, the host cannot cache pages from blocks in SLC and the default mode in the same RANDOM READ CACHE (00h-31h) operation. The host has to wait until an operation on a block in the default mode is complete before starting an operation on a block in SLC mode and vice versa.

When performing multi-plane operations, all the blocks which are being accessed must be in the same mode (i.e. SLC or default mode).

If the host controller uses a structured data pattern to program a page or pages of a NAND block when in SLC mode, then the NAND host is required to appropriately randomize the data and program the entire page length (i.e. all columns) even if beyond the user data.

3Bh Operation Guidelines

1. **Atomic Operation:** The host will treat the SLC entry sequence (SLC MODE LUN ENABLE (3Bh) + Array_operation) as an atomic operation i.e. the host is not allowed to issue any other command (except Reset command) between SLC Entry Opcode and array operation. When WP# is Low, and command 3Bh is issued and is followed by a Program/Erase operation or an invalid array operation, it will not be executed by the NAND. The part will revert to TLC state.
2. **RESET:** If a host issues RESET (FFh, FAh) at any time during the Prefix SLC entry, (even if reset command is issued immediately after issuing SLC MODE LUN ENABLE (3Bh), then NAND will go into TLC mode and resets SLC entry command SLC MODE LUN ENABLE (3Bh). The host shall reenter the entire sequence for SLC entry in this case.
3. **Multi-Plane:** In multi-plane array operation, the LUN address from the first plane sequence is used to enter the SLC mode.
4. **Multi-LUN:** In a Multi-LUN system, when using SLC entry command, host shall complete the command sequence on a particular LUN before issuing commands on other LUN. For example, if a host issues multi-plane command on LUN0 with SLC entry opcode as prefix, then host shall finish the multi-plane command sequence on LUN0 before operating on non-LUN0. Command 3Bh needs to be issued before entering into SLC OTF mode for any LUN, even during interleaved operation. Upon SLC operation completion, each LUN will revert to TLC mode.
   a) Example SLC OTF operation during Interleaved operations. Note that Only LUN A will program the block in SLC Mode and revert to TLC mode after the operation is completed, and LUN B would perform the program operation in TLC mode.
      i) SLC MODE LUN ENABLE (3Bh)
      ii) Program Page (80h-10h) on LUN A
      iii) While SR[6] is low, PROGRAM PAGE (80h-10h) on LUN B

   b) Example SLC OTF operation during Interleaved operations. Note that LUN A will program the block in SLC Mode and revert to TLC mode after the operation is competed, and LUN B would perform the program operation in SLC Mode and revert to TLC mode after the operation is competed.
      i) SLC MODE LUN ENABLE (3Bh)
      ii) PROGRAM PAGE (80h-10h) on LUN A
      iii) While SR[6] is low, SLC MODE LUN ENABLE (3Bh) + PROGRAM PAGE (80h-10h)

5. **Status Command:** READ STATUS (70h/71h/78h/79h) commands are not allowed while the host is performing the SLC entry or exit command sequence.
6. ***IWL Mixed Mode Read:*** IWL Mixed Mode Read is allowed. 3Bh command is accepted during SR[6:5] = 10. A 3Bh prefix command followed by IWL READ (00h-20h) command will be executed only if addressed plane group is ready. A 3Bh prefix command followed by IWL READ (00h-20h) command to a busy plane group will be ignored and the existing operation will continue.
   a) IWL Mixed Mode Read Case (Prefix 3Bh followed by IWL READ (00h-20h) command)
      i) Plane Group X is idle, Plane Group Y is idle: 3Bh command (Prefix 3Bh is accepted by both Plane Groups); 00h-20h command to Plane Group X (Plane Group X goes into SLC mode, Plane Group Y is reset (not addressed plane).
      ii) Plane Group X is idle, Plane Group Y is busy: 3Bh command (Prefix 3Bh is accepted by Plane Group X and is ignored by Plane Group Y(busy)); 00h-20h command to Plane Group X (Plane Group X goes into SLC mode, Plane Group Y continues existing operation.)
      iii) Plane Group X is busy, Plane Group Y is idle: 3Bh command (Prefix 3Bh is ignored by Plane Group X and accepted by Plane Group Y); 00h-20h command to Plane Group X (Plane Group X ignores 3Bh command sequence and continues existing operation, Plane Group Y is reset (not addressed plane).

iv) Plane Group X is busy, Plane Group Y is busy: 3Bh command (Prefix 3Bh is ignored by Plane Group X (busy) and is ignored by Plane Group Y (busy)); 00h-20h command to Plane Group X (Plane Group X ignores 3Bh command sequence and continues existing operation, Plane Group Y ignores 3Bh command sequence and continues existing operation.

b) Example of IWL Mixed Mode read while LUN is idle
   i) SLC MODE LUN ENABLE (3Bh) + IWL READ (00h-20h) (Block Q Page R) (Plane Group 1 - SLC Mode) (Plane Group 2 = idle TLC mode)
   ii) Note that if Plane Group 2 is idle, 3Bh is accepted by both Plane Groups but is reset upon 00h-20h for unselected plane group.
   iii) SLC MODE LUN ENABLE (3Bh) + IWL READ (00h-20h) (Block Q Page S) (Plane Group 1 - SLC Mode)
   iv) Note that if Plane Group 2 is idle, 3Bh is accepted by both Plane Groups but is reset upon 00h-20h for unselected plane group.
   v) SLC MODE LUN ENABLE (3Bh) + IWL READ (00h-20h) (Block X Page A) (Plane Group 1 - SLC Mode)
   vi) Note that if Plane Group 2 is idle, 3Bh is accepted by both Plane Groups but is reset upon 00h-20h for unselected plane group.
   vii) IWL READ (00h-20h) (Plane Group 2 - Block Y Page L) (Plane Group 2 - TLC Mode)
   viii) SLC MODE LUN ENABLE (3Bh) + IWL READ (00h-20h) (Block X Page B) (Plane Group 1 - SLC Mode)
   ix) SLC MODE LUN ENABLE (3Bh) + IWL READ (00h-20h) (Block X Page C) (Plane Group 1 - SLC Mode)
   x) IWL READ (00h-20h) (Block Z Page H) (Plane Group 2 - TLC Mode)
   xi) Wait for ARDY = 1 (Plane Group 1)
   xii) TLC operation to Plane Group 1 (Both Plane Groups in TLC Mode)
   xiii) IWL READ (00h-20h) (Block A Page F) (Plane Group 1 - TLC Mode)
   xiv) SLC MODE LUN ENABLE (3Bh) + IWL READ (00h-20h) (Block B Page W) (Plane Group 2 - SLC Mode)
   xv) SLC MODE LUN ENABLE (3Bh) + IWL READ (00h-20h) (Block B Page X) (Plane Group 2 - SLC Mode)
   xvi) IWL READ (00h-20h) (Block A Page F) (Plane Group 1 - TLC Mode)
   xvii) Wait for ARDY = 1 (Plane Group 2)
   xviii) TLC operation to Plane Group 2 (Both Plane Groups in TLC Mode)

c) Example of IWL Mixed Mode read while LUN is in an active program or erase
   i) Multi-Plane Program (Erase)
   ii) Program (Erase) Suspend
   iii) SLC MODE LUN ENABLE (3Bh) + IWL READ (00h-20h) (Block X Page A) (Plane Group 1 - SLC Mode)
   iv) IWL READ (00h-20h) (Plane Group 2 - Block Y Page L) (Plane Group 2 - TLC Mode)
   v) SLC MODE LUN ENABLE (3Bh) + IWL READ (00h-20h) (Block X Page B) (Plane Group 1 - SLC Mode)
   vi) SLC MODE LUN ENABLE (3Bh) + IWL READ (00h-20h) (Block Y Page R) (Plane Group 1 - SLC Mode)
   vii) SLC MODE LUN ENABLE (3Bh) + IWL READ (00h-20h) (Block X Page D) (Plane Group 1 - SLC Mode)
   viii) IWL READ (00h-20h) (Block Y Page M) (Plane Group 2 - TLC Mode)
   ix) SLC MODE LUN ENABLE (3Bh) + IWL READ (00h-20h) (Block A Page E) (Plane Group 1 - SLC Mode)
   x) IWL READ (00h-20h) (Block C Page N) (Plane Group 2 - TLC Mode)

xi) Wait for ARDY = 1 (Plane Group 1)
xii) TLC operation to Plane Group 1 (Both Plane Groups in TLC Mode)
xiii) Program (Erase) Resume

7. **Cache:** During Cache operation in both Read and Program, LUN address associated with the first cache command will enter the SLC mode. If 3Bh command is not issued, the LUN will revert back to TLC mode at end of the previous cache Read/Program operation i.e. ARDY=1. 3Bh command is accepted during SR[6:5] = 10. Since 31h has no block address, the host is responsible to ensure that the same block is being read with the same mode. The host is responsible to pair 3Bh with 31h.
   a) Example of Cache Program:
      i) SLC MODE LUN ENABLE (3Bh) + Cache Program (LUN A - Page A) puts LUN-A into SLC mode
      ii) SLC MODE LUN ENABLE (3Bh) +Cache Program (LUN A - Page B) in SLC mode
      iii) SLC MODE LUN ENABLE (3Bh) +Cache Program (LUN A - Page C) in SLC mode
      iv) ...
      v) SLC MODE LUN ENABLE (3Bh) +Cache Program (LUN A - Page N) in SLC mode
      vi) Wait for ARDY = 1
      vii) TLC operation to LUN A
   b) Example of READ CACHE SEQUENTIAL (31h):
      i) SLC MODE LUN ENABLE (3Bh) + READ PAGE (00h-30h)
      ii) SLC MODE LUN ENABLE (3Bh) + READ PAGE CACHE SEQUENTIAL (31h)
      iii) SLC MODE LUN ENABLE (3Bh) + READ PAGE CACHE SEQUENTIAL (31h)
      iv) 3Fh (To close out a Cache Read operation)
      v) Wait for ARDY = 1
      vi) TLC operation to LUN A
   c) Example of READ PAGE CACHE RANDOM (00h-31h):
      i) SLC MODE LUN ENABLE (3Bh) + READ PAGE (00h-30h)
      ii) SLC MODE LUN ENABLE (3Bh) + READ PAGE CACHE RANDOM (00h-31h)
      iii) SLC MODE LUN ENABLE (3Bh) + READ PAGE CACHE RANDOM (00h-31h)
      iv) 3Fh (To close out a Cache Read operation)
      v) Wait for ARDY = 1
      vi) TLC operation to LUN A
8. **Suspends:** The host can suspend a TLC Program or Erase operation to perform SLC operation and similarly SLC operation can be suspended to perform TLC operation. When the suspend command is issued during Program or Erase operation, the NAND records the device state in which suspend occurred. When Resume command is issued, NAND will switch to the mode in which it was suspended based on the stored information. Host needs to be aware that NAND will put device back in a state (TLC or SLC) in which it was suspended. NAND will automatically exit SLC mode following the SLC operation. This includes the suspend operation i.e. if a suspend operation occurs in SLC mode then LUN is put in TLC mode after the suspend operation occurred.
9. **Nested Suspend:** As an extension to Program or Erase suspend, host can perform nested suspend while switching the mode from TLC to SLC. Similar to Program or Erase Suspend, NAND will track the suspended state and resume back in the same mode.

Example sequence for Suspend operations:

1. TLC Program/Erase Suspend:
   a) Program/Erase LUN0 (TLC)
   b) Suspend Program/Erase LUN0 (NAND stores suspended state)

c) SLC MODE LUN ENABLE (3Bh) + Read (r_SLC) - LUN0 exits SLC mode after the array operation
d) Program/Erase Resume LUN0 (TLC)

2. SLC Program/Erase Suspend :
   a) Program/ Erase LUN0 (SLC) (Example: 3Bh + 80h-10h)
   b) Suspend Prog/Erase LUN0 (NAND stores suspended state and exits SLC mode) (Example: 84h)
   c) TLC Read operation (Example: 00h-30h)
   d) Program/Erase Resume (NAND restores the LUN0 into SLC mode before starting resume operation) (Example: 13h)

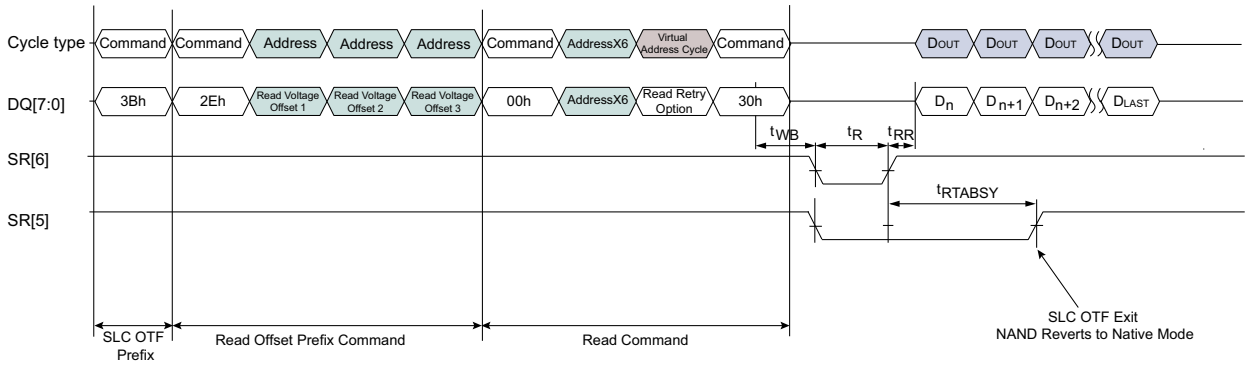
3. TLC Nested Suspend:
   a) Erase LUN0 (TLC)
   b) Suspend Erase LUN0 (NAND stores suspended state)
   c) SLC MODE LUN ENABLE (3Bh) SLC_entry + Program LUN0 (SLC)
   d) Suspend Program (NAND stores suspended state and exits SLC mode)
   e) TLC Read operation
   f) Program Resume (NAND restores the LUN0 into SLC mode before starting resume operation)
   g) Erase Resume (NAND restores the LUN0 into TLC mode before starting resume operation)

Prefix Opcode for SLC Entry

Prefix Opcode for SLC entry provides a host the fastest way to enter SLC mode on the fly (OTF). The NAND will automatically revert to TLC mode at the end of the SLC array operation when ARDY is 1. This provides system with flexibility and reduced complexity in managing the SLC blocks.

To change the mode of a NAND LUN from TLC mode to SLC, the host issues SLC MODE LUN ENABLE (3Bh) followed by a valid SLC array operation. Then the LUN address provided in the array addressing enters SLC mode at the array confirm command and array operation occurs in the SLC mode.

Figure 96: READ OFFSET PREFIX (2Eh) SLC OTF Sequence



Valid Operations with SLC MODE LUN ENABLE (3Bh)

The valid operations following SLC MODE LUN ENABLE (3Bh) are listed in the table below. The general rules for 3Bh operation are that the 3Bh command followed by an allowed command will result

in a valid operation in SLC mode. Expected behavior should follow these rules if they are not listed in Valid Operations with SLC MODE LUN ENABLE (3Bh) table.

Table 68: Valid Operations with SLC MODE LUN ENABLE (3Bh)

Group	Operation	SLC MODE LUN ENABLE (3Bh) command result
Read Operations	3Bh + Read Series operation (00h-30h, 00h-35h, 00h-20h)	Valid operation in SLC
	3Bh + READ CACHE RANDOM (00h-31h)	Valid operation in SLC
	3Bh + READ PAGE CACHE SEQUENTIAL (31h)	Valid operation in SLC
	3Bh + READ PAGE CACHE LAST (3Fh)	Ignored
	3Bh + READ PAGE MULTI-PLANE (00h-32h)	Valid operation(s) in SLC
	3Bh + IWL READ (00h-20h) Mixed Mode	Valid operation(s) in SLC
	3Bh + SBSBR (00h-34h)	Valid operation in SLC
Read Offset Prefix Operations (2Eh)	3Bh + 2Eh + Read Series operation (00h-30h, 00h-35h, 00h-20h)	Valid operation in SLC
	3Bh + 2Eh + READ CACHE RANDOM (00h-31h)	Valid operation in SLC
	3Bh + 2Eh + READ PAGE CACHE SEQUENTIAL (31h)	Valid operation in SLC
	3Bh + 2Eh + READ PAGE CACHE LAST (3Fh)	Ignored
	3Bh + 2Eh + READ PAGE MULTI-PLANE (00h-32h)	Valid operation(s) in SLC
	3Bh + 2Eh + IWL READ (00h-20h) Mixed Mode	Valid operation(s) in SLC
Program Operations	3Bh + PROGRAM PAGE (80h-10h) Single Plane operation	Valid operation in SLC
	3Bh + PROGRAM PAGE CACHE (80h-15h)	Valid operation in SLC
	3Bh + PROGRAM PAGE MULTI-PLANE (80h-11h)	Valid operation(s) in SLC
	3Bh + COPYBACK PROGRAM (85h-10h)	Valid operation in SLC
	3Bh + COPYBACK PROGRAM MULTI-PLANE (85h-11h)	Valid operation(s) in SLC
Erase Operations	3Bh + ERASE BLOCK (60h-D0h)	Valid operation in SLC
	3Bh + ERASE BLOCK MULTI-PLANE (60h-60h-D0h)	Valid operation(s) in SLC
WP# Low	3Bh + Read Operation	Valid operation in SLC
Reset Operation	3Bh + RESET Command (FFh, FAh)	Valid operation(s) in SLC

Table 69: NAND Mode for SLC Entry with Auto Exit Option

Operation	Valid commands	NAND mode - entry	NAND mode - exit
		ARDY = 0	ARDY 0 to 1
SLC Program	3Bh + 80h-add -10h/11h	SLC	TLC [2]
	3Bh + 85h-add - 10h/11h		
SLC Read	3Bh + 00h-add-30h/32h/20h	SLC	TLC [2]
	3Bh + 2Eh-offsets-00h-add-30h/32h/20h		

Table 69: NAND Mode for SLC Entry with Auto Exit Option (Continued)

Operation	Valid commands	NAND mode - entry	NAND mode - exit
		ARDY = 0	ARDY 0 to 1
SLC Erase	3Bh + 60h-add-D0h	SLC	TLC [2]
	3Bh + 60h-add-D1h		
SLC Program Suspend	84h	N/A	TLC
Program Resume	13h	TLC or SLC[1]	TLC
SLC Erase Suspend	61h	N/A	TLC
Erase Resume	D2h	TLC or SLC [1]	TLC

Notes: 1. TLC/SLC entry occurs after ARDY 1 –> 0 transition.
2. For multi-plane program/read/erase, NAND goes back to TLC mode only after the final command is given.

TLC One Pass Programming

Program operations are used to move data from the cache or data registers to the NAND array of one or more planes. In TLC One Pass programming, the lower page data, upper page data, and eXtra page data are programmed simultaneously into the array. For MLC page One Pass programming, lower page data and upper page data are programmed simultaneously into the array. For SLC page programming, lower page data only is programmed into the array.

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (that is, 0, 1, 2, 3, …). Programming pages out of order within a block is prohibited.

If RESET (FFh, FAh) is issued anytime during the program sequence prior to ^{t}PROG time (including ^{t}PBSY time), the program sequence is aborted and must be restarted from the beginning. Data in the data register is valid.

The following commands are allowed during data input of the One Pass Programming operation; IWL READ (00h-20h), READ PAGE (00h-30h), COPYBACK READ (00h-35h), READ PAGE MULTI-PLANE (00h-32h), and SINGLE BIT SOFT BIT READ (SBSBR) (00h-34h). During allowed read operations, it is possible to use the READ OFFSET PREFIX (2Eh) Command and ACRR (enabled by Feature Address 96h). All ERASE operations, Cache read operations, and AUTO READ CALIBRATION (Feature Address 96h) are prohibited.

It is also prohibited to issue any programming commands to other blocks in the same plane after data entry has begun. If any prohibited command is issued during data entry of a programming operation the host is required to start the programming operation over again from the beginning.

The One Pass Programming mode supports the Program Clear functionality as defined by P1[6] of Feature Address 01h.

PROGRAM SUSPEND (84h) and PROGRAM RESUME (13h) operations are supported during One Pass Programming operation.

MLC Single Pass Programming Operations

When the MLC Single Pass programming algorithm is selected, both lower and upper page data must be entered before data is programmed into the array. Lower page data must be entered before the upper page data. After data has been entered to a lower page address, the confirm command will trigger the LUN to move the data from the cache register into the data register. After data has been entered to an upper page address, the confirm command will trigger the LUN to begin the program operation.

The PROGRAM PAGE (80h-10h) command is used to enter the lower page address and data into the cache register. A PROGRAM PAGE (80h-10h) command sequence is only allowed to be issued to a die (LUN) when its RDY = 1 and ARDY =1. After the 10h command is entered the LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PBSY while data is transferred from the cache register into the data register. A second PROGRAM PAGE (80h-10h) operation is used to enter the upper page address and data into the cache register. After the 10h command is entered the LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PROG while data is written to the array. If RESET (FFh, FAh) is issued anytime during the program sequence prior to ^{t}PROG time (including ^{t}PBSY time), the program sequence is aborted and must be re-started from the beginning. Data in the page registers is valid.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit.

It is the responsibility of the host to ensure that the lower page and upper page address are on a shared wordline. No internal address checks are performed by the LUN. In the event that the lower page and upper page addresses are not on a shared wordline, the data will be programmed to the lower and upper pages of the wordline specified by the upper page address.

The host is not allowed to issue a PROGRAM PAGE (80h-10h) command to an upper page without previously entering an 80h-10h command to a lower page. If a second PROGRAM PAGE (80h-10h) command is issued with a lower page address, the data from the first lower page address will be overwritten. A subsequent (80h-10h) command sequence with upper page address and data will still be required to trigger the start of the program algorithm.

For pages that are mapped by default as SLC (edge of block or SLC blocks) only a single PROGRAM PAGE (80h-10h) operation is required. The die (LUN) will recognize the page addressed is in SLC mode and begin the programming operation after the confirm command (10h) is issued.

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can also be used with single pass programming enabled. A PROGRAM PAGE MULTI-PLANE (80h-11h) command is allowed when RDY = 1 and ARDY = 0 during program cache operations. Otherwise, a PROGRAM PAGE MULTI-PLANE (80h-11h) command is only allowed to be issued to a die (LUN) when its RDY = 1 and ARDY =1. Special care must be taken to ensure the command sequence follows the correct order when multi-plane programming operations are being used. Because the LUN is triggered to move data from the cache register into the data register only after the confirm command (10h) associated with data loaded to a lower page address, data must first be loaded into the lower page of each plane before upper page data can be loaded. Multi-Plane operations follow all of the same restrictions as single-plane operations.

Example command sequence for PROGRAM PAGE with Single Pass Programming Enabled:

1. Issue PROGRAM PAGE (80h-10h) with lower page data
2. Wait ^{t}PBSY
3. Issue PROGRAM PAGE (80h-10h) with upper page data
4. Wait ^{t}PROG

Example command sequence for PROGRAM PAGE MULTI-PLANE with Single Pass Programming Enabled (2 Planes):

1. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 lower page data
2. Wait ^{t}DBSY
3. Issue PROGRAM PAGE (80h-10h) with Plane 1 lower page data
4. Wait ^{t}PBSY
5. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 upper page data
6. Wait ^{t}DBSY
7. Issue PROGRAM PAGE (80h-10h) with Plane 1 upper page data
8. Wait ^{t}PROG

Figure 97: PROGRAM PAGE (80h-10h) Operation with MLC Single Pass Programming

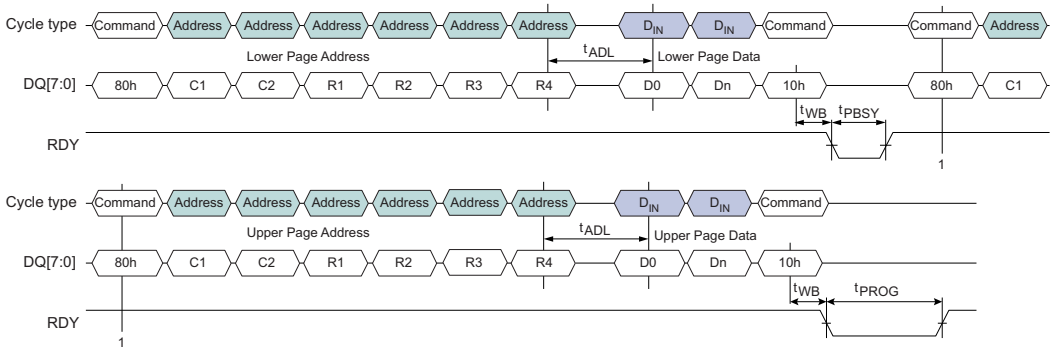
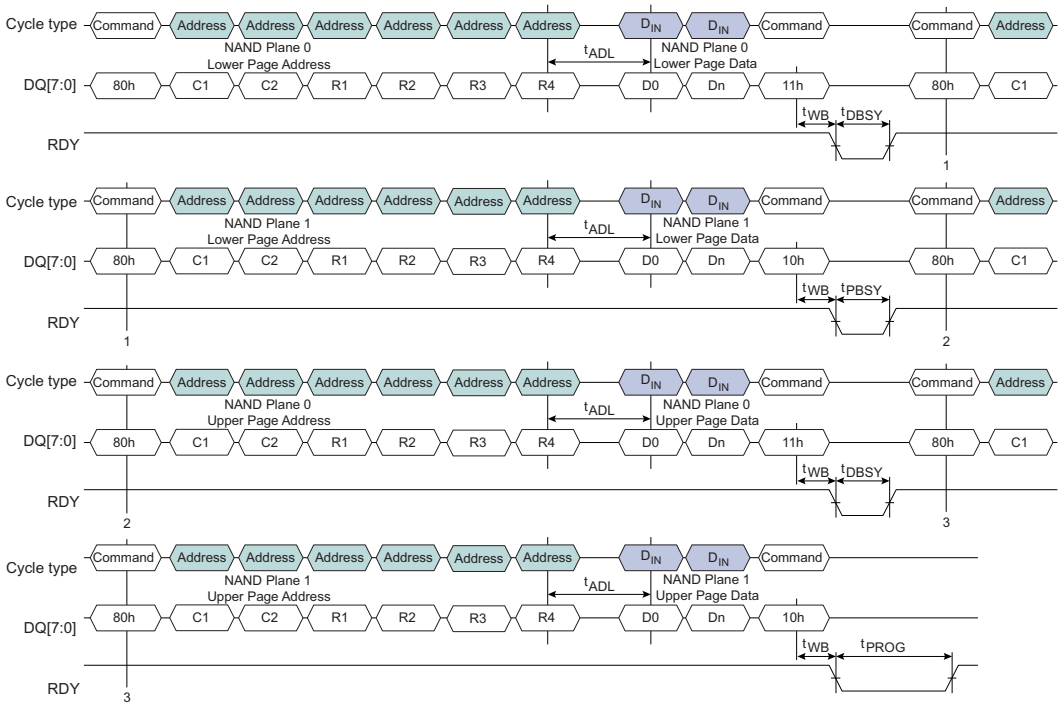


Figure 98: Two-Plane PROGRAM PAGE MULTI-PLANE (80h-11h) Operation with MLC Single Pass Programming



Program Operations

The Program Operation using the PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and move the data from the cache register to the specified block and page address in the array of the selected die (LUN).

Program Cache Operations

The PROGRAM PAGE CACHE (80h-15h) command can be used to improve program operation system performance. When this command is issued, the die (LUN) goes busy (RDY = 0, ARDY = 0) while the cache register contents are copied to the data register, and the die (LUN) is busy with a program cache operation (RDY = 1, ARDY = 0). While the contents of the data register are moved to the NAND Flash array, the cache register is available for an additional PROGRAM PAGE CACHE (80h-15h) command. PROGRAM PAGE (80h-10h) commands are not supported as the confirm command in a Cache

Programming sequence that starts the array program operation, only the PROGRAM PAGE CACHE (80h-15h) command is supported for the confirm command in a Cache Programming sequence.

For PROGRAM PAGE CACHE-series (80h-15h) operations, during the die (LUN) busy times, ^{t}CBSY and ^{t}LPROG, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 71h, 78h) and RESET (FFh, FAh). When RDY = 1 and ARDY = 0, the only valid commands during PROGRAM PAGE CACHE-series (80h-15h) operations are status operations (70h, 71h, 78h), PROGRAM PAGE CACHE (80h-15h), CHANGE WRITE COLUMN (85h), CHANGE ROW ADDRESS (85h), and RESET (FFh, FAh).

Multi-Plane Program Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve program operation system performance by enabling multiple pages to be moved from the cache registers to different planes of the NAND Flash array. Multi-Plane operations follow all of the same restrictions as single-plane operations. See Multi-Plane Operations for details.

Multi-Plane Program Cache Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve program cache operation system performance by enabling multiple pages to be moved from the cache registers to the data registers and, while the pages are being transferred from the data registers to different planes of the NAND Flash array, free the cache registers to receive data input from the host. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE CACHE (80h-15h) command. See Multi-Plane Operations for details.

PROGRAM PAGE (80h-10h)

The PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and move the data from the cache register to the specified block and page address in the array of the selected die (LUN). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

For TLC One Pass programming, the lower page data must be entered first, followed by the upper page data, and then the eXtra page data. The PROGRAM PAGE (80h-10h) command is used to enter the lower page address and data into the cache register. Unless preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. After the 80h command, write the required address cycles containing the column address and row address of the lower page address. Data input cycles follow after the lower page address. The host data is sequentially entered starting at the column address specified. At any time during the data input cycle, the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. After the data input is complete, write the confirm command 10h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}PBSY while the lower page data is transferred from the cache register into the data register.

After the lower page data has been entered, the One Pass programming requires the upper page data to be entered next. The host is not allowed to program an Upper Page directly without entering Lower Page prior to it. When the LUN's status indicates it is ready (RDY = 1, ARDY = 1), the same sequence that was used for entering the lower page address is repeated for the upper page address. After the upper page data input is complete, write the confirm command 10h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}PBSY while the upper page data is transferred from the cache register into the data register.

After the upper page data has been entered, the One Pass programming requires the eXtra page data to be entered. The host is not allowed to program an eXtra Page directly without entering Lower Page and Upper Page prior to it. When the LUN's status indicates it is ready (RDY = 1, ARDY = 1), the same sequence that was used for entering the lower and the upper page addresses are repeated for the eXtra page address. After the data input is complete, write the confirm command 10h to the command

register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for tPROG while the lower page data, upper page data, and eXtra page data are programmed into the array simultaneously. It is the responsibility of the host to ensure that the lower page, upper page, and eXtra page addresses are on the shared pages. No internal address checks are performed by the LUN. In the event that the lower page address, upper page address, and eXtra page address are not on the shared pages, then the lower page data, upper page data, and eXtra page data will not be valid.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 71h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit.

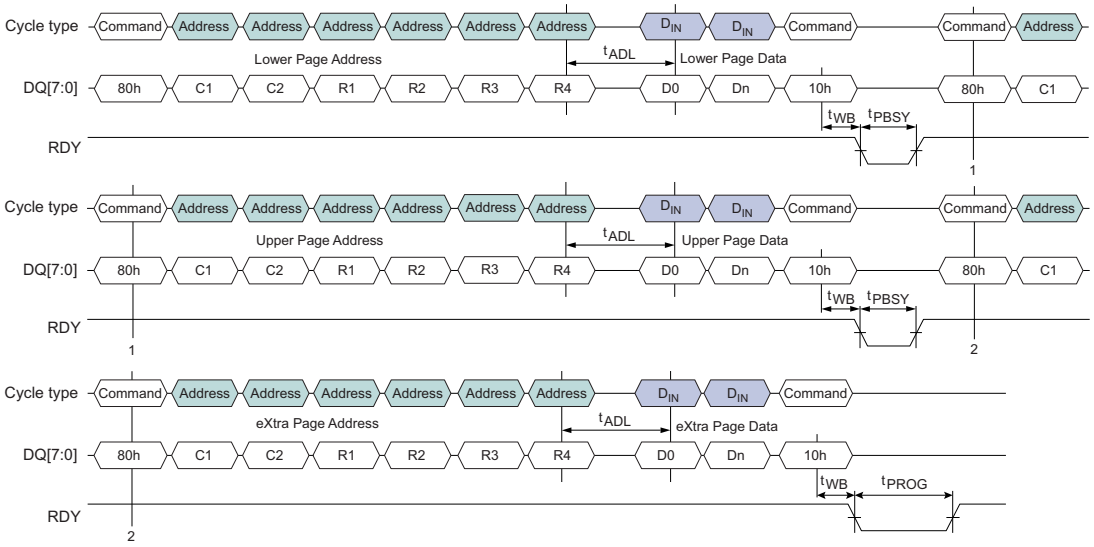
In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS (71h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

When the last PROGRAM PAGE (80h-10h) command is used as the final command of a multi-plane program operation, it is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands, data is transferred from the cache registers for all of the addressed planes to the NAND array. The host should check the status of the operation by using the status operations (70h, 71h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Example command sequence for PROGRAM PAGE (80h-10h) - TLC One Pass:

1. Issue PROGRAM PAGE (80h-10h) with lower page data
2. Wait tPBSY
3. Issue PROGRAM PAGE (80h-10h) with upper page data
4. Wait tPBSY
5. Issue PROGRAM PAGE (80h-10h) with eXtra page data
6. Wait tPROG

Figure 99: PROGRAM PAGE (80h-10h) Operation - TLC One Pass



PROGRAM PAGE CACHE (80h-15h)

The PROGRAM PAGE CACHE (80h-15h) command enables the host to input data to a cache register; copies the data from the cache register to the data register; then moves the data register contents to the

specified block and page address in the array of the selected die (LUN). When performing cache programming operations, only a single PROGRAM PAGE CACHE (80h-15h) operation can be entered during Cache Busy (^{t}CBSY) time (RDY = 1, ARDY = 0). After the single PROGRAM PAGE CACHE (80h-15h) operation, data will not be transferred from the cache register into the data register until the cache program operation in progress is completed (RDY = 1, ARDY = 1). After the data is copied to the data register, the cache register is available for additional PROGRAM PAGE CACHE (80h-15h) commands. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that the operation has completed successfully.

In TLC One Pass programming, the lower page data must be entered first, followed by the upper page data, and then the eXtra page data. The PROGRAM PAGE CACHE (80h-15h) command is used to enter the lower page address and data into the cache register. Unless preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. After 80h command, write the required address cycles containing the column address and row address of the lower page address. Data input cycles follow after the lower page address. The host data is sequentially entered starting at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 15h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PBSY as the lower page data is transferred.

After the lower page data has been entered, the One Pass programming requires the upper page data to be entered next. The host is not allowed to program an Upper Page directly without entering Lower Page prior to it. When the LUN's status indicates it is ready (RDY = 1), the same sequence that was used for entering the lower page address is repeated for the upper page address. When data input is complete, write 15h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PBSY as the upper page data is transferred.

After the upper page data has been entered, the One Pass programming requires the eXtra page data to be entered. The host is not allowed to program an eXtra Page directly without entering Lower Page and Upper Page prior to it. When the LUN's status indicates it is ready (RDY = 1), the same sequence that was used for entering the lower and the upper page addresses are repeated for the eXtra page address. When data input is complete, write 15h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}CBSY as the lower page data, upper page data, and eXtra page are programmed simultaneously into the array. This allows the data register to become available for the next cache program operation.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 71h, 78h) can be used. When the LUN's status shows that it is busy with a PROGRAM CACHE operation (RDY = 1, ARDY = 0), the host should check the status of the FAILC bit to see if a previous cache operation was successful.

If, after ^{t}CBSY, the host wants to wait for the program cache operation to complete, without issuing the PROGRAM PAGE CACHE (80h-15h) command, the host should monitor ARDY until it is 1. The host should then check the status of the FAIL and FAILC bits.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS (71h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

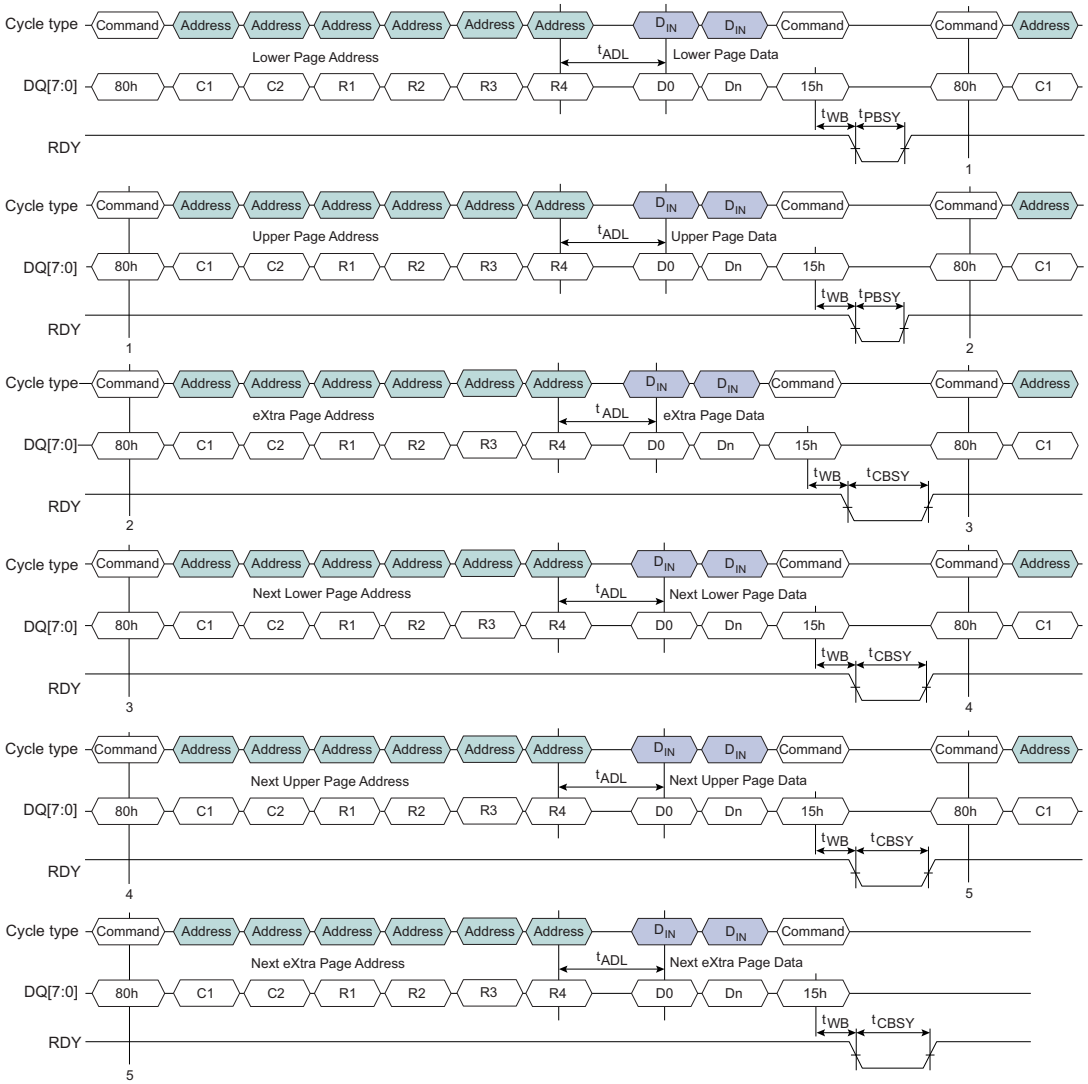
The PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a multi-plane program cache operation. It is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands. Data for all of the addressed planes is transferred from the cache registers to the corresponding data registers, then moved to the NAND Flash array. The host should check the status of the

operation by using the status operations (70h, 71h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Example command sequence for PROGRAM PAGE CACHE (80h-15h) (Start) - TLC One Pass:

1. Issue PROGRAM PAGE CACHE (80h-15h) with lower page data
2. Wait ^{t}PBSY
3. Issue PROGRAM PAGE CACHE (80h-15h) with upper page data
4. Wait ^{t}PBSY
5. Issue PROGRAM PAGE CACHE (80h-15h) with eXtra page data
6. Wait ^{t}CBSY
7. Issue PROGRAM PAGE CACHE (80h-15h) with next lower page data
8. Wait ^{t}CBSY
9. Issue PROGRAM PAGE CACHE (80h-15h) with next upper page data
10. Wait ^{t}CBSY
11. Issue PROGRAM PAGE CACHE (80h-15h) with next eXtra page data
12. Wait ^{t}CBSY

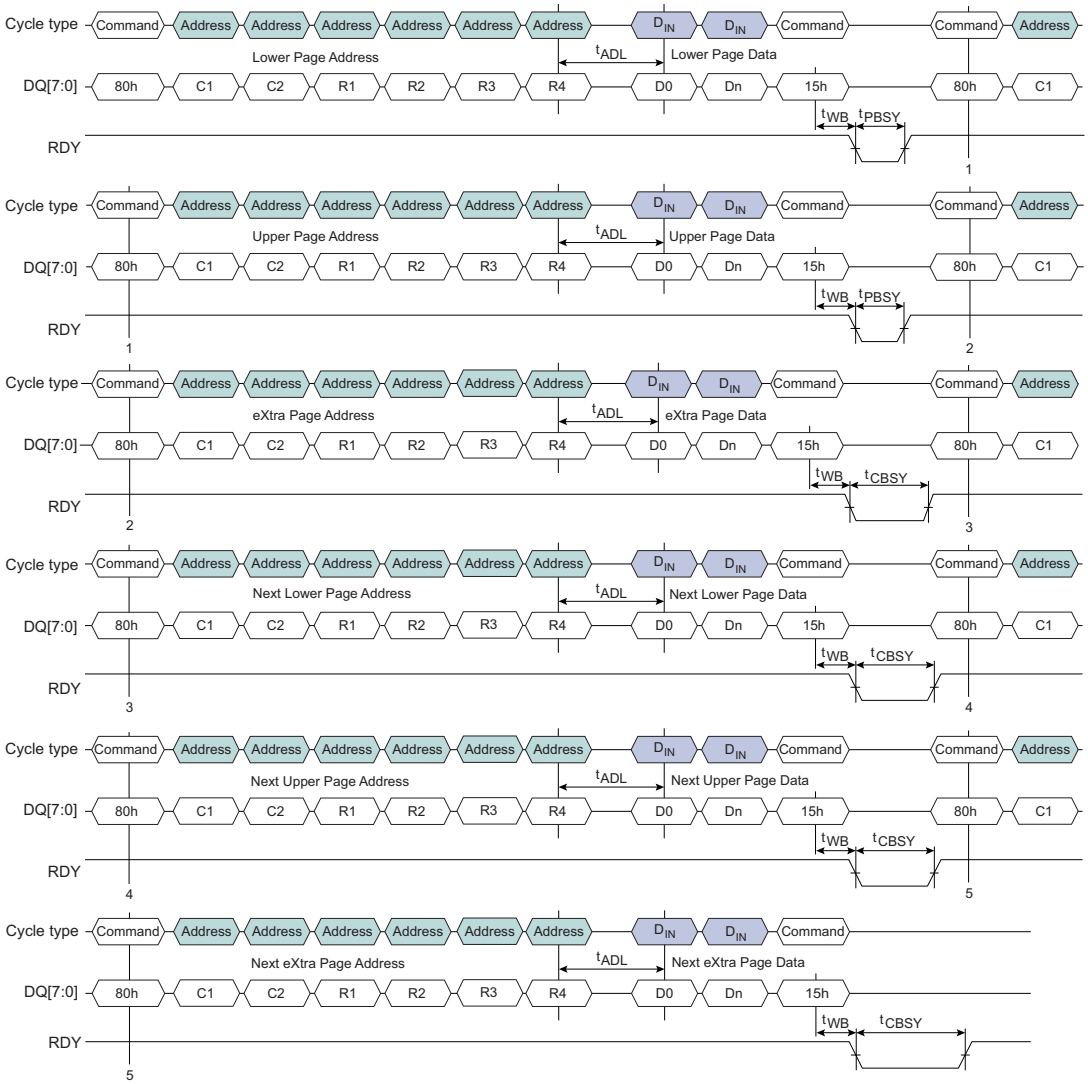
Figure 100: PROGRAM PAGE CACHE (80h-15h) Operation (Start) - TLC One Pass



Example command sequence for PROGRAM PAGE CACHE (80h-15h) (End) - TLC One Pass:

1. Issue PROGRAM PAGE CACHE (80h-15h) with lower page data
2. Wait ^{t}PBSY
3. Issue PROGRAM PAGE CACHE (80h-15h) with upper page data
4. Wait ^{t}PBSY
5. Issue PROGRAM PAGE CACHE (80h-15h) with eXtra page data
6. Wait ^{t}CBSY
7. Issue PROGRAM PAGE CACHE (80h-15h) with next lower page data
8. Wait ^{t}CBSY
9. Issue PROGRAM PAGE CACHE (80h-15h) with next upper page data
10. Wait ^{t}CBSY
11. Issue PROGRAM PAGE CACHE (80h-15h) with next eXtra page data
12. Wait ^{t}CBSY (status bit ARDY will be LOW for ^{t}LPROG for the last 15h command)

Figure 101: PROGRAM PAGE CACHE (80h-15h) Operation (End) - TLC One Pass



PROGRAM PAGE MULTI-PLANE (80h-11h)

The PROGRAM PAGE MULTI-PLANE (80h-11h) command enables the host to input data to the addressed plane's cache register and queue the cache register to ultimately be moved to the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the program operation for all previously queued planes, issue either the PROGRAM PAGE (80h-10h) command or the PROGRAM PAGE CACHE (80h-15h) command. All of the queued planes will move the data to the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY =1, ARDY =1 for non-cache programming operations and RDY=1, ARDY=1 or 0 during cache programming). Special care must be taken to ensure the command sequence follows the correct order when multi-plane programming operations are being used. Because the die (LUN) is triggered to move data from the cache register into the data register only after the confirm command (10h or 15h), data must first be loaded into the lower page of each plane before the data for all upper page addresses, followed by data for all eXtra page addresses. Multi-Plane operations follow all of the same restrictions as single-plane operations.

In TLC One Pass programming, the lower page data of each plane must be entered first, followed by the upper page data of each plane, and then the eXtra page data of each plane. The PROGRAM PAGE MULTI-PLANE (80h-11h) command is used to enter the lower page address and data into the cache register of the first NAND plane. Unless immediately preceded by an 11h command; with the exception of status operations (70h, 71h, 78h), issuing the 80h to the command register clears all of the cache registers' contents on non-busy LUNS on the selected target. After 80h command, write the required address cycles containing the column address and row address for a lower page to the first NAND plane. Data input cycles follow after the lower page address of the associated NAND plane. The host data is sequentially entered starting at the column address specified. At any time during the data input cycle, the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY. When the LUN's status shows that it is ready (RDY =1, ARDY =1 for non-cache programming operations and RDY=1, ARDY=1 or 0 during cache programming) and the lower page data entry is committed for the first NAND plane, write another 80h to the command register and then write the required address cycles containing the column address and row address of the lower page address of subsequent NAND plane.

Additional PROGRAM PAGE MULTI-PLANE (80h-11h) commands can be issued to queue additional planes of lower page addresses for data transfer in this manner.

To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 71h, 78h) can be used.

When the last address of lower page plane data is desired to be issued, the PROGRAM PAGE (80h-10h) shall be issued instead of the PROGRAM PAGE MULTI-PLANE (80h-11h). The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PBSY.

After the lower page data has been entered, the One Pass programming requires the upper page data to be entered next. The host is not allowed to program an Upper Page directly without entering Lower Page prior to it. When the LUN's status shows that it is ready (RDY =1, ARDY =1 for non-cache programming operations and RDY=1, ARDY=1 or 0 during cache programming), the same sequence that was use for entering the lower page addresses for the previous inputted number of planes is repeated for the upper page addresses. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY. When the last address of upper page plane data is desired to be issued, the PROGRAM PAGE (80h-10h) shall be issued instead of the PROGRAM PAGE MULTI-PLANE (80h-11h). The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PBSY.

After the upper page data has been entered, the One Pass programming requires the eXtra page data to be entered. The host is not allowed to program an eXtra Page directly without entering Lower Page and Upper Page prior to it. When the LUN's status shows that it is ready (RDY =1, ARDY =1 for non-cache programming operations and RDY=1, ARDY=1 or 0 during cache programming), the same sequence that was use for entering the lower and upper page addresses for the previous inputted number of planes is repeated for the eXtra page addresses. When data input is complete, write 11h to the command register. When the last address of eXtra page plane data is desired to be issued, the PROGRAM PAGE (80h-10h) shall be issued instead of the PROGRAM PAGE MULTI-PLANE (80h-11h). When the final PROGRAM PAGE (80h-10h) command in issued with the last eXtra page addresses, data is transferred from the cache registers to the NAND Flash array for all of the addressed planes for lower, upper and eXtra pages during ^{t}PROG. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit for each of the planes to verify that programming completed successfully.

When the PROGRAM PAGE CACHE (80h-15h) command is used in place of the PROGRAM PAGE (80h-10h) command, the final command of a MULTI-PLANE PROGRAM CACHE operation, data is

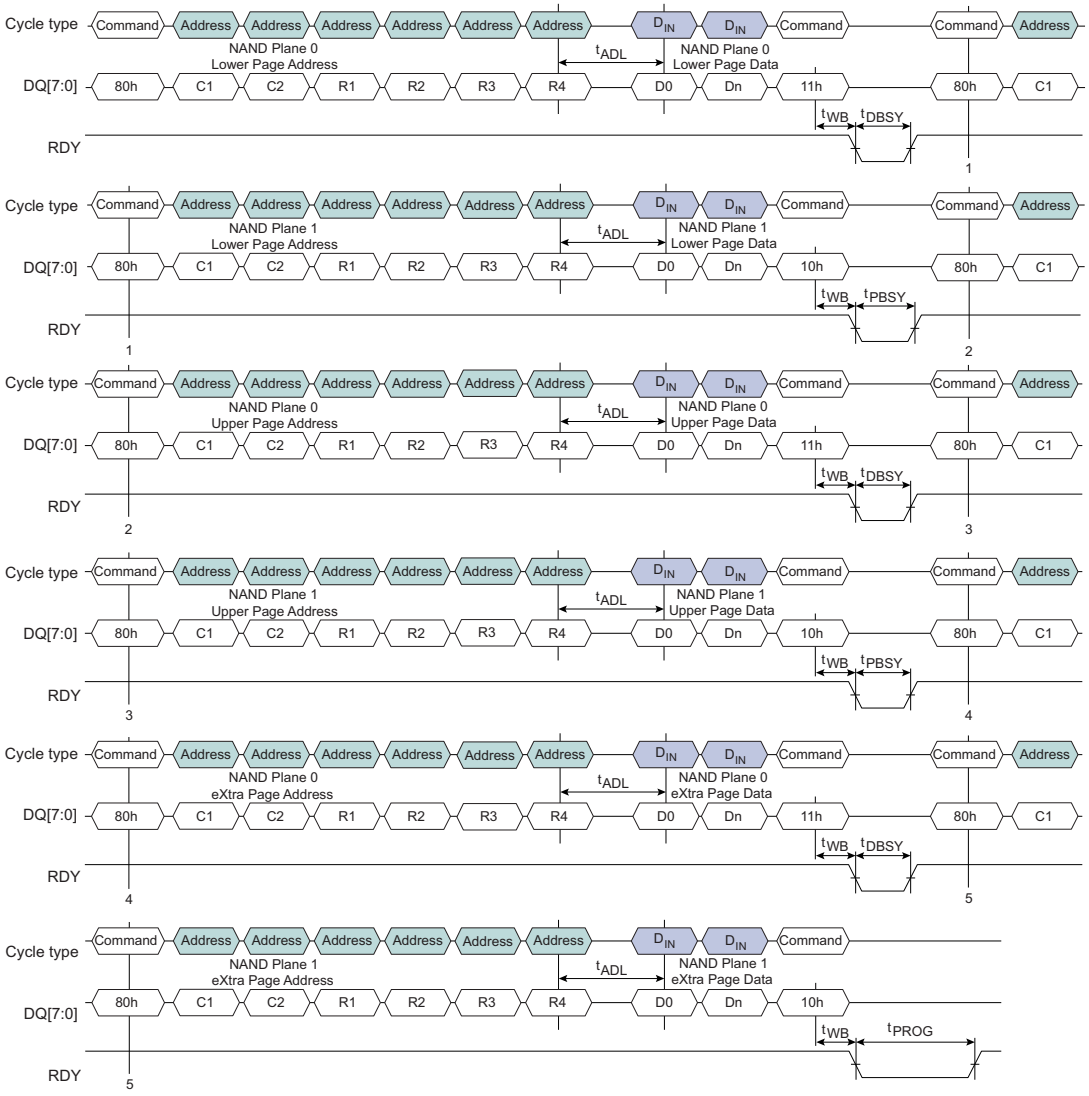
transferred from the cache registers to the data registers after the previous array operations finish. The data is then moved from the data registers to the NAND Flash array for all of the addressed planes. This occurs during ^{t}CBSY. After ^{t}CBSY, the host should check the status of the FAILC bit for each of the planes from the previous program cache operation, if any, to verify that programming completed successfully.

For the PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE (80h-10h), and PROGRAM PAGE CACHE (80h-15h) commands, see Multi-Plane Operations for multi-plane addressing requirements.

Example command sequence for PROGRAM PAGE MULTI-PLANE (80h-11h) - TLC One Pass (2-Planes):

1. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 lower page data
2. Wait ^{t}DBSY
3. Issue PROGRAM PAGE (80h-10h) with Plane 1 lower page data
4. Wait ^{t}PBSY
5. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 upper page data
6. Wait ^{t}DBSY
7. Issue PROGRAM PAGE (80h-10h) with Plane 1 upper page data
8. Wait ^{t}PBSY
9. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 eXtra page data
10. Wait ^{t}DBSY
11. Issue PROGRAM PAGE (80h-10h) with Plane 1 eXtra page data
12. Wait ^{t}PROG

Figure 102: Two-Plane PROGRAM PAGE MULTI-PLANE (80h-11h) Operation - TLC One Pass

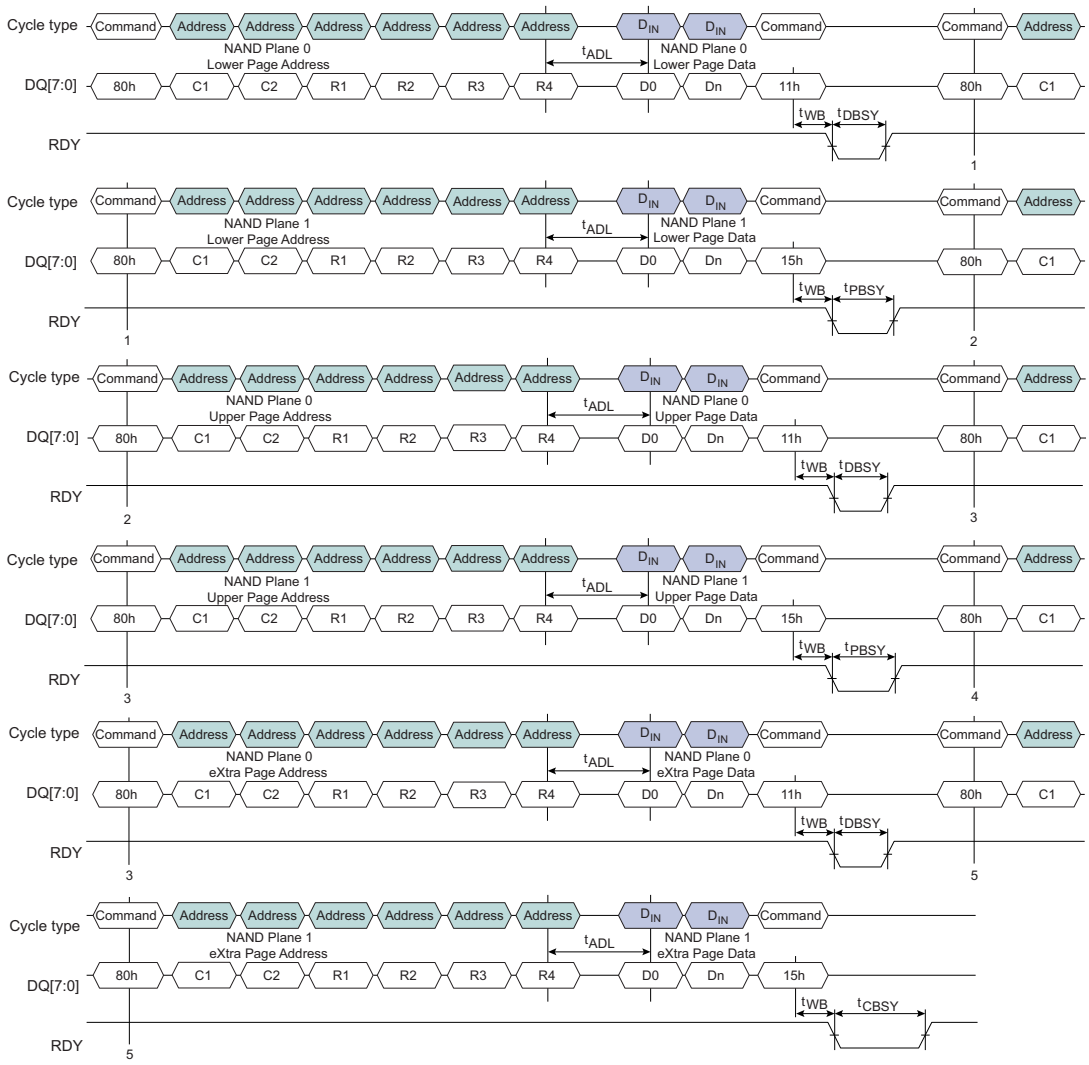


Example command sequence for PROGRAM PAGE MULTI-PLANE (80h-11h) combined with PROGRAM PAGE CACHE (80h-15h) (End) - TLC One Pass (2-Planes):

1. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 lower page data
2. Wait ^{t}DBSY
3. Issue PROGRAM PAGE CACHE (80h-15h) with Plane 1 lower page data
4. Wait ^{t}PBSY
5. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 upper page data
6. Wait ^{t}DBSY
7. Issue PROGRAM PAGE CACHE (80h-15h) with Plane 1 upper page data
8. Wait ^{t}PBSY
9. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 eXtra page data
10. Wait ^{t}DBSY
11. Issue PROGRAM PAGE CACHE (80h-15h) with Plane 1 eXtra page data

12.Wait tCBSY
13.Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with next Plane 0 lower page data
14.Wait tDBSY
15.Issue PROGRAM PAGE CACHE (80h-15h) with next Plane 1 lower page data
16.Wait tCBSY
17.Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with next Plane 0 upper page data
18.Wait tDBSY
19.Issue PROGRAM PAGE CACHE (80h-15h) with next Plane 1 upper page data
20.Wait tCBSY
21.Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with next Plane 0 eXtra page data
22.Wait tDBSY
23.Issue PROGRAM PAGE (80h-15h) with next Plane 1 eXtra page data
24.Wait tCBSY (status bit ARDY will be LOW for tLPROG for the last 15h command)

Figure 103: Two-Plane PROGRAM PAGE MULTI-PLANE (80h-11h) with PROGRAM PAGE CACHE (80h-15h) Operation (End) - TLC One Pass



PROGRAM SUSPEND (84h) and PROGRAM RESUME (13h)

The PROGRAM SUSPEND (84h) command is used to pause a program in execution for the LUN specified (RDY = 0, ARDY = 0 or RDY = 1, ARDY = 0). If a PROGRAM SUSPEND (84h) command is issued when RDY (SR [6]) is set to one or zero and ARDY (SR [5]) is set to one or zero and the LUN is not performing a program operation, then the PROGRAM SUSPEND (84h) command should be ignored (that is, ^{t}PSPDN = 0, R/B# stays HIGH). If the host issues a PROGRAM SUSPEND (84h) while there is no program operation ongoing (including the case of the LUN already being in a program suspend state with SR[3] = 1), the command should be ignored (that is, ^{t}PSPDN = 0, R/B# stays HIGH). If a multi-plane program is executing, the program operation for all multi-plane addresses is paused and the LUN shall make forward progress for the program operation prior to suspending the operation. The LUN shall make forward progress for the program prior to suspending provided the delay from the PROGRAM RESUME (13h) to the subsequent PROGRAM SUSPEND (84h) command is longer than ^{t}RSPSPD. Note that ^{t}RSPSPD is defined as the minimum time required for EVERY program pulse to make forward progress regardless of the number of pulses allowed/required. Issuing a PROGRAM SUSPEND (84h) command after a PROGRAM RESUME (13h) with a delay shorter than ^{t}RSPSPD is not recommended but is allowed, but there may not be forward progress in the suspended program operation. Regardless of forward progress, a single program operation may not be suspended more than 30 times. If a delay is used which is shorter than ^{t}RSPSPD it cannot be guaranteed that the program operation will complete before reaching the maximum allowed suspend operations, and if the maximum allowed number of suspends is reached then the full remaining ^{t}PROG time must be allowed to complete without any further suspend operations. The host shall resume the operation by issuing PROGRAM RESUME (13h) within ^{t}SUSPEND_P of issuing PROGRAM SUSPEND (84h). When using program suspend, the observed ^{t}PROG may exceed ^{t}PROG (Max).

The PROGRAM SUSPEND (SR[3]) bit of the status register is valid for this command after ARDY transitions from zero to one and until the suspended program is resumed or RESET (FFh, FAh, FDh) is issued. The FAIL (SR[0]) bit of the status register is valid for this command after ARDY transitions from zero to one until the next transition of ARDY to zero. PROGRAM SUSPEND (SR[3]) shall be set to one if a program was suspended successfully, in this case FAIL (SR[0]) shall be cleared to zero. SR[3] shall be cleared to zero if the program was completed, in this case SR[0] reflects whether the program was successful.

The host shall not toggle WP# low on any target that has suspended program operation.

Table 70: PROGRAM SUSPEND (84h) Status Details

Description	SR[3][1]	SR[1]	SR[0]
PROGRAM completed with successful status	0	Previous program or erase fail status	0
PROGRAM completed with fail status	0	Previous program or erase fail status	1
PROGRAM suspended	1	X (invalid)	X (invalid)

Notes: 1. Program Suspend SR[3] is persistent and will always reflect if a program is suspended on the LUN. SR[3] = 1 is valid after a Program Suspend [84h] command and ARDY transitions from zero to one until the suspended program is resumed or RESET (FFh, FAh, FDh) is issued.

To suspend an ongoing program operation to a LUN, issue 84h command, then write the required address cycles containing the row address (LUN, block and page addresses) and column address. Only the LUN address is required for program suspend; the block, page, and column addresses are ignored. The selected LUN status will be reflected in the status bits FAIL (SR[0]) and PROGRAM SUSPEND (SR[3]) in the status register after the status bit RDY is set to one. The selected LUN which the program operation was suspended on will respond within ^{t}PSPD.

To resume a suspended program operation to a LUN, issue 13h command, then write the required address cycles containing the row address matching the LUN in the suspended state; the block, page, and column addresses are ignored. The suspended program operation will then resume and finish within ^{t}PROG.

While a program is suspended, if the host issues a RESET (FFh, FAh, FDh) command for the affected LUN, then the program that was suspended is canceled and status is cleared. The ^{t}RST time that will elapse during this operation is ^{t}RST during program since it is actively cancelling a program suspend operation. With the exception of Erase and Program commands, all commands are accepted during suspended state (some with limitations listed in subsequent paragraphs). Additionally, READ UNIQUE ID (EDh), READ OTP PAGE, and READ PARAMETER PAGE (ECh) operations are not allowed when a LUN on that target is in a program suspend state.

SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands are permitted during program suspend (including nested suspend), refer to Restrictions During Suspend State for details on Feature Address supported during suspend.

Cache read and auto read calibration are not allowed when LUN is in a program suspend state. While in program suspend state, SBSBR and READ OFFSET PREFIX (2Eh) command can be used to recover error bits.

While a program is suspended, if host issues a Read (00h-20h, 00h-30h, 00h-35h) based command to the page address (or shared pages) of the suspended program the read will be performed with data output being undefined and the program that was suspended keeps its suspend state. If host issues read command to block or LUN address other than the suspended page address then the read is performed and the program that was suspended keeps its suspend state.

If the host issues a PROGRAM SUSPEND (84h) while there is no program operation ongoing the command should be ignored (that is, ^{t}PSPD = 0, R/B# stays HIGH). If the host issues a PROGRAM RESUME (13h) while there is no program operation ongoing or no program suspended, the NAND will respond with a ^{t}PSPDN busy time and the LOCK status (SR[7] = 0) is set (SR[3], SR[2], SR[1], and SR[0] will be "don't care"), SR[4] is reset, ESR[1] and ESR[0] will not change. If the host issues a PROGRAM SUSPEND (84h) to a LUN already in program suspend state the command will be ignored and the program that was suspended will stay in the program suspend state.

During SLC cache program, if PROGRAM SUSPEND (84h) is issued afer PROGRAM PAGE CACHE (80h-15h) confirm command on the next page data entry, the current program operation is allowed to finish. Upon PROGRAM RESUME (13h), the next program operation on the queue will start. This sequence may result in longer ^{t}PSPD than normal as the current program is allowed to finish when the PROGRAM SUSPEND (84h) command is issued after the PROGRAM PAGE CACHE (80h-15h) command. This NAND behavior also applies to non-native mode WL's (that is, SLC WL on a TLC block).

During cache program, if a PROGRAM SUSPEND (84h) is issued, SR[4] is invalid until PROGRAM RESUME (13h) is issued. Thermal alert status may be monitored directly using the EXTENDED STATUS REGISTER READ (79h) command.

Program suspend operations are only supported in the default mode of operation (that is, not in the OTP mode of operation).

See Restrictions During Suspend State for Valid Operations during Program Suspend.

Figure 104: PROGRAM SUSPEND (84h) Operation

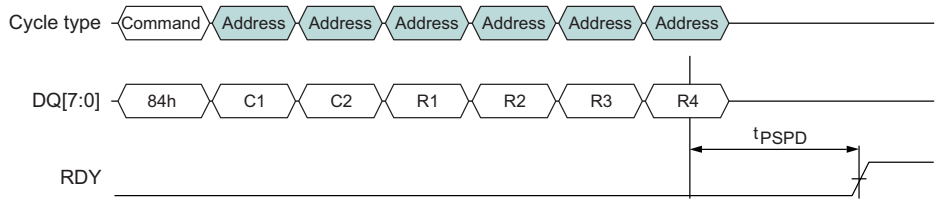
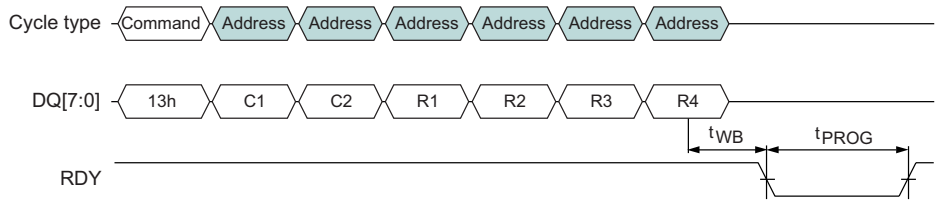


Figure 105: PROGRAM RESUME (13h) Operation



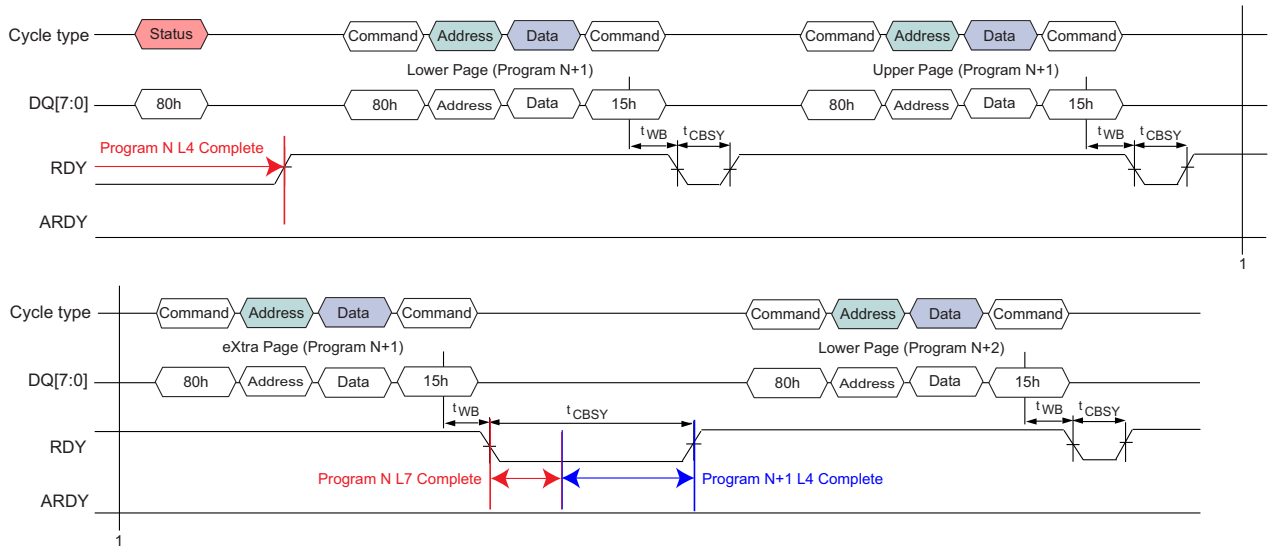
Multiple Page Data Entry during Cache Programming

There were limitations for cache programming on the previous NAND designs, where only one page (per plane) of data could be entered during the RDY = 1 and ARDY = 0 state. After the single page is entered, RDY = 0 until the current program operation is completely finished.

For performance improvement, it is now allowed to enter multiple pages of data, for up to three pages, during the RDY = 1 and ARDY = 0 state in cache programming.

To enable Multiple Page Data Entry during Cache Programming, a 15h command is required after each page data entry. Please note 10h command is not accepted for the Multiple Page Data Entry during Cache Programming. In contrast to the previous NAND designs, both 10h and 15h command are accepted for cache programming, with the requirement of a 15h command on the final page data entry to initiate the cache programming operation.

Figure 106: Multiple Page Data Entry during Cache Programming



Feature Address 7Fh: Manual Dynamic Word Line Start Voltage

Manual Dynamic Word Line Start Voltage (MDWLSV) provides a method to keep ^{t}PROG consistently close to spec ^{t}PROG for partially programmed blocks (open blocks) by allowing the host to store the wordline start voltage. The host can store the offset values for an extended set of open blocks based on system capability and need.

Dynamic Word Line Start Voltage (DWLSV) is a feature to optimize ^{t}PROG throughout the lifetime of the device, by evaluating the program speed and adjusts the Word Line Start Voltage (WLSV). Early in life when programming speed is typically slower, it is possible to increase the WLSV to reduce the required programming time. Later in the endurance lifetime when the programming speed is faster, it is possible to use the default WLSV to achieve the same overall ^{t}PROG.

DWLSV can be applied to both TLC and SLC blocks but not to SLC/MLC edge WLs in a TLC block.

- The programming speed and the associated WLSV are evaluated internally on the first page of a TLC wordline in a TLC block. The WLSV offset is then stored internally on the NAND and can be used for the subsequent pages in the TLC wordline in a TLC block. Since the WLSV offset is resampled at the first page of the following TLC wordline, the ^{t}PROG for the first page of a TLC wordline will always have a longer ^{t}PROG, since no WLSV information is available which results in the use of the default program start voltage.
- The programming speed and the associated WLSV are evaluated internally on the first page of a SLC wordline in a SLC block. The WLSV offset is then stored internally on the NAND and can be used for the subsequent pages in the SLC wordline in a SLC block. Since the WLSV offset is resampled at the first page of the following SLC wordline, the ^{t}PROG for the first page of a SLC wordline will always have a longer ^{t}PROG, since no WLSV information is available which results in the use of the default program start voltage.
- A block configured in SLC OTF mode would require a different offset than the same block configured in TLC mode. If the block configuration has been changed, the host is responsible for applying the correct offset.

This WLSV offset generated by the NAND device can now be retrieved and stored by the host by issuing GET FEATURES by LUN (D4h) command to FA = 7Fh P3, the host can then apply this WLSV offset by issuing SET FEATURES by LUN (D5h) to FA = 7Fh P1. This offset can be applied for all subsequent pages in the TLC/SLC wordline to adjust the WLSV, hence to achieve the optimized ^{t}PROG on partially programmed blocks (open blocks).

Setting FA = 7Fh P1 does not guarantee immediate program operation will observe faster ^{t}PROG, as the NAND may be at the first page of a wordline. The host is responsible for storing the WLSV offsets for a given partially programmed block (open block) by using the GET FEATURE by LUN (D4h) of the NAND generated WLSV offset in FA = 7Fh P3. This Sub-Feature P3 value will be used for the subsequent page programming. When the host returns to program a partially programmed block that has the WLSV offsets stored, the host must provide the offset values using SET FEATURES by LUN (D5h) to FA = 7Fh P1 prior to programming in order to achieve the optimal ^{t}PROG performance. After programming of the page, the NAND will populate Sub-Feature P3 with the new sampled value (if user page is the first page of a wordline) or the Sub-Feature P1 value provided by the host. Feature Address 7Fh Sub Feature P1 will still contain the last issued user offset.

If the DWLSV offset information is not available, the default WLSV will be used and DWLSV sampling will happen on the first page that is programmed.

The MDWLSV information is reset when a RESET (FFh, FAh, FDh) command is issued. Feature Address 7Fh sub-feature parameter output after a GET FEATURES by LUN (D4h) command will be P1=FFh,

P2=P3=P4=00h. The program following a reset operation will automatically resample unless a SET FEATURE by LUN (D5h) to FA = 7Fh P1 is issued prior to the program operation.

Regarding multi-plane programming, FA = 7Fh P3 will be populated with the lowest offset value (from the fastest to program block) among the blocks programmed. Blocks within a multi-plane program group must remain the same during multi-plane programming. No mixing of different blocks from different multi-plane program groups is allowed. User cannot sample a single plane program offset value and use it for a multi-plane program operation.

Cache Programming has same function as Non-Cache Programming for MDWLSV. GET FEATURE by LUN (D4h) and SET FEATURE by LUN (D5h) will be accepted when RDY=1. Value will be retrieved and updated by NAND before releasing RDY.

Table 71: Feature Address 7Fh: Manual Dynamic Word Line Start Voltage

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1 - Get Feature by LUN (D4h) / Set Feature by LUN (D5h)											
Host Applied WLSV Offset		–	–	–	–	–	–	–	–		
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3 - Get Feature by LUN (D4h) Only											
NAND Generated WLSV Offset		–	–	–	–	–	–	–	–		
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. MDWLSV only supports GET FEATURE by LUN (D4h) and SET FEATURE by LUN (D5h). GET FEATURE (EEh) and SET FEATURE (EFh) are invalid.
2. Set Feature by LUN (D5h) values of FFh or 00h to FA = 7Fh P1 is an illegal operation.
3. Array reliability will not be guaranteed if the host inputs non-NAND generated values into Feature Address 7Fh P1[7:0]. The host shall only input NAND generated values into Feature Address 7Fh P1[7:0]. If correct DSV information is unknown/lost, DO NOT load any value into Feature Address 7Fh P1[7:0].
4. If Feature Address 7Fh Sub-Feature P1 is set before a new block program, P1 value takes precedence over P3 value for a new block program when switching between blocks.

Figure 107: Example Sequence for Programming between Blk A and Blk B - MDWLSV only Storing Offset for Blk A

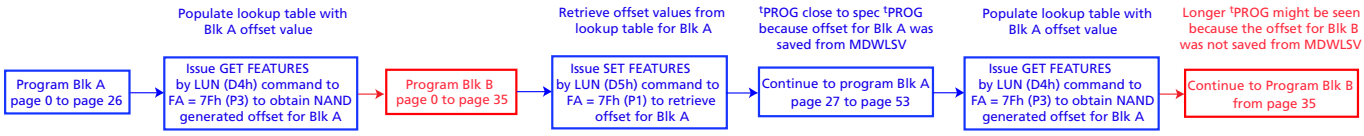
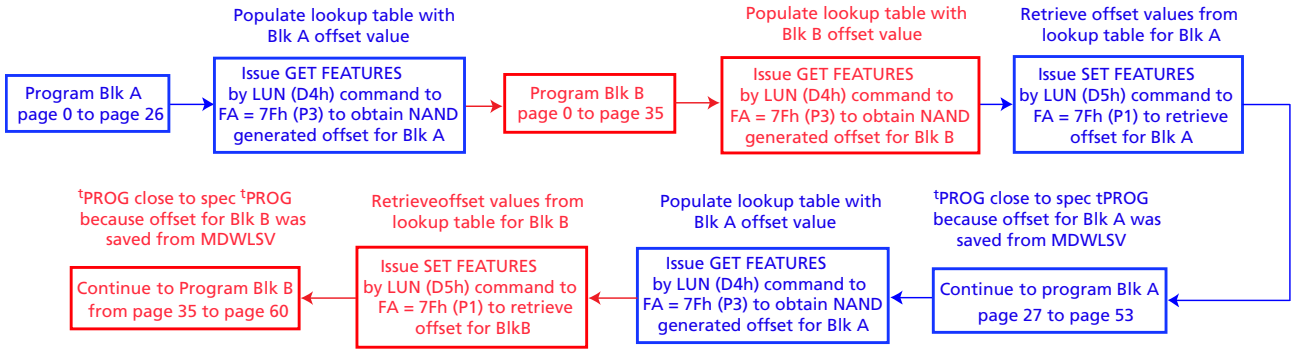


Figure 108: Example Sequence for Programming between Blk A and Blk B - MDWLSV Storing Offsets for both Blk A and Blk B



Erase Operations

Erase operations are used to clear the contents of a block in the NAND Flash array to prepare its pages for program operations.

Erase Operations

The ERASE BLOCK (60h-D0h) command, when not preceded by the ERASE BLOCK MULTI-PLANE (60h-D1h) command, erases one block in the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

MULTI-PLANE ERASE Operations

The ERASE BLOCK MULTI-PLANE (60h-D1h) command can be used to further system performance of erase operations by allowing more than one block to be erased in the NAND array. This is done by prepending one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands in front of the ERASE BLOCK (60h-D0h) command. See Multi-Plane Operations for details.

ERASE BLOCK (60h-D0h)

The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

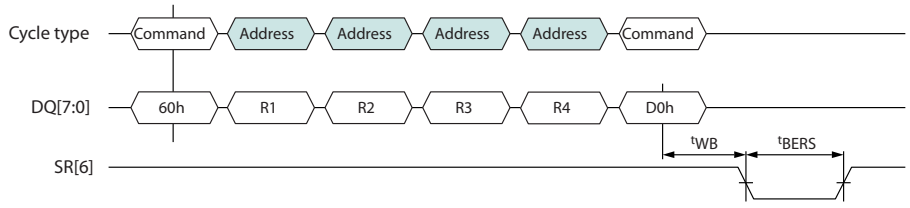
To erase a block, write 60h to the command register. Then write the required address cycle input; the page address is ignored. Conclude by writing D0h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}BERS while the block is erased.

To determine the progress of an ERASE operation, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 71h, 78h) can be used. When the die (LUN) is ready (RDY = 1, ARDY = 1) the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the FIXED ADDRESS READ STATUS (71h) or READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The ERASE BLOCK (60h-D0h) command is used as the final command of a MULTI-PLANE ERASE operation. It is preceded by one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands. All of the blocks addressed by the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) command sequence will be erased. The host should check the status of the operation by using the status operations (70h, 71h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Figure 109: ERASE BLOCK (60h-D0h) Operation



ERASE BLOCK MULTI-PLANE (60h-D1h)

The ERASE BLOCK MULTI-PLANE (60h-D1h) command queues a block in the specified plane to be erased in the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for a block to be erased. To specify the final block

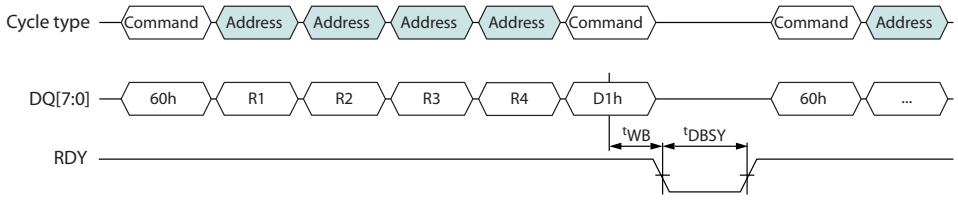
to be erased and to begin the ERASE operation for all previously queued planes, issue the ERASE BLOCK (60h-D0h) command. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To queue a block to be erased, write 60h to the command register, then write the required address cycle input; the page address is ignored. Conclude by writing D1h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 71h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1, ARDY = 1), additional ERASE BLOCK MULTI-PLANE (60h-D1h) commands can be issued to queue additional planes for erase. Alternatively, the ERASE BLOCK (60h-D0h) command can be issued to erase all of the queued blocks.

For multi-plane addressing requirements for the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Multi-Plane Operations.

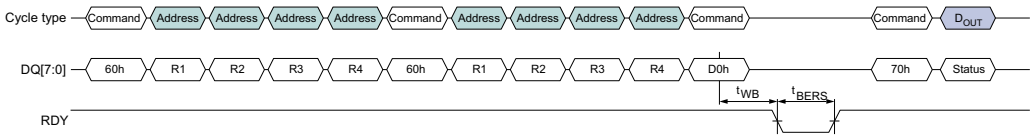
Figure 110: ERASE BLOCK MULTI-PLANE (60h–D1h) Operation



ERASE BLOCK MULTI-PLANE (60h-60h-D0h)

This operation behaves the same as the ERASE BLOCK MULTI-PLANE (60h-D1h) command followed by a ERASE BLOCK (60h-D0h) command.

Figure 111: ERASE BLOCK MULTI-PLANE (60h–60h-D0h) Operation



ERASE SUSPEND (61h) and ERASE RESUME (D2h)

The ERASE SUSPEND (61h) command is used to pause an erase in execution for the LUN specified (RDY = 0, ARDY = 0). If ERASE SUSPEND (61h) is issued when ARDY = 1 or 0 and LUN is not performing an erase operation then the ERASE SUSPEND (61h) command should be ignored (that is, ^{t}ESPD = 0). If an interleaved erase is executing (erase operations on more than one LUN on a target), the erase for the addressed LUN with the ERASE SUSPEND (61h) command is paused. The LUN shall make forward progress for the erase prior to suspending (e.g. complete an erase pulse) provided the delay from the ERASE RESUME (D2h) to the subsequent ERASE SUSPEND (61h) command is longer than ^{t}RSESPD. Note that ^{t}RSESPD is defined as the minimum time required for EVERY erase pulse to make forward progress regardless of the number of pulses allowed/required. Issuing an ERASE SUSPEND (61h) command after an ERASE RESUME (D2h) with a delay shorter than ^{t}RSESPD is not recommended but is allowed, but there may not be forward progress in the suspended erase operation. Regardless of forward progress, a single erase operation may not be suspended more than 30 times (i.e. it is allowed for a mix of delays longer and shorter than ^{t}RSESPD. If a delay is used which is shorter than ^{t}RSESPD it

cannot be guaranteed that the erase operation will complete before reaching the maximum allowed suspend operations, and if the maximum allowed number of suspends is reached then the full remaining ^{t}BERS time must be allowed to complete without any further suspend operations. The host shall resume the operation by issuing ERASE RESUME (D2h) or ERASE BLOCK (60h-D0h) within ^{t}SUSPEND_E of issuing ERASE SUSPEND (61h).

The host shall not toggle WP# low on any target that has suspended erase operations or nested suspend operations.

FAIL (SR[0]) and ERASE SUSPEND (SR[2]) of the status register are valid for this command after RDY transitions from zero to one until the next array operation transition of RDY to zero. SR[2] shall be set to one if an erase was suspended successfully, in this case SR[0] shall be cleared to zero. SR[2] shall be cleared to zero if the erase was completed, in this case SR[0] reflects whether the erase was successful.

To suspend a ongoing erase operation to a LUN, write 61h to the command register, then write the required address cycle input; the block and page addresses are ignored. Only the LUN address is used for erase suspend. The selected LUN status will be reflected in the status bits FAIL (SR[0]) and ERASE SUSPEND (SR[2]) in the status register after the status bit RDY (SR[6]) is set to one.

Table 72: ERASE SUSPEND (61h) Status Details

Description	SR[2][1]	SR[1]	SR[0]
ERASE completed with successful status	0	Previous program or erase fail status	0
ERASE completed with fail status	0	Previous program or erase fail status	1
ERASE suspended[2]	1	X (invalid)	X (invalid)

Notes: 1. Erase Suspend SR[2] is persistent and will always reflect if an erase is suspended on the LUN. SR[2] = 1 is valid after an Erase Suspend [61h] command and ARDY transitions from zero to one until the suspended erase is resumed or RESET (FFh, FAh, FDh) is issued.
2. See Nested Suspend section for status details during nested erase suspend.

For multi-plane addressing requirements for the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Multi-Plane Operations.

To resume a suspended erase operation issue the ERASE RESUME (D2h) or ERASE BLOCK (60h-D0h) command to the target (CE#)/LUN which has had an erase operation suspended. The suspended erase operation will then resume and finish within ^{t}BERS. In the case of Multi-LUN erase operations that have been suspended, the ERASE RESUME (D2h) command will cause all LUNs on a target (CE#) to resume any suspended erase operations. However, if issuing ERASE BLOCK (60h-D0h) command to that target (CE#) instead, only the addressed LUN will resume its suspended erase operation.

While an erase is suspended, if the host issues a RESET (FFh, FAh, FDh) command for the affected LUN then the erase that was suspended is canceled and status is cleared. The ^{t}RST time that will elapse during this operation is ^{t}RST during erase since it is actively cancelling an erase suspend operation. Commands READ UNIQUE ID (EDh), READ OTP PAGE, and READ PARAMETER PAGE (ECh) are not allowed when the LUN is in an erase suspend state. All other commands are accepted during suspended state (some with limitations listed in subsequent paragraphs). SET FEATURES (EFh) and SET FEATURES BY LUN (D5h) commands are permitted during erase suspend.

While an erase is suspended, if host issues a ERASE BLOCK (60h-D0h) command to the suspended block the suspended erase will be resumed (not restarted) and the erase that was suspended is canceled and status is cleared. If block erase is issued to different block address than suspended block then the erase is performed on the selected block and the erase that was suspended is canceled and

status is cleared. If an erase is issued to a different LUN on the shared target then the erase is performed on the selected block and the erase that was suspended keeps its suspend state.

Table 73: ERASE SUSPEND (61h) Behavior for ERASE Operations

Description	Command Issued	Next State
Block A erase operation suspended	ERASE BLOCK to Block A	Resume erase operation to Block A
	ERASE BLOCK to Block B	Start normal erase to Block B and suspend to Block A is canceled
	ERASE BLOCK MULTI-PLANE to Block A and B	Start normal erase to Block A and B
ERASE BLOCK MULTI-PLANE to Block A and B suspended	ERASE BLOCK to Block A	Resume erase operation to Block A and B
	ERASE BLOCK to Block B	Resume erase operation to Block A and B
	ERASE BLOCK MULTI-PLANE to Block A and B	Resume erase operation to Block A and B
	ERASE BLOCK MULTI-PLANE to Block A and D	Start normal erase to block A and D. Suspend to Block B is canceled
	ERASE BLOCK MULTI-PLANE to Block C and B	Start normal erase to block C and B. Suspend to Block A is canceled

While an erase is suspended, if host issues a program command to the suspended block or in the case of multi-plane program, if at least one of the blocks addressed has a suspended erase, the program is aborted with short busy time (^{t}ESPDN) and the LOCK status (SR[7] = 0) is set. In this case, the erase that was suspended keeps it's suspend state and can still be resumed. If host issues a program command to a block or LUN address other than the suspended block, also in case of a multi-plane program operation, as long as the suspended block is not one of the addressed blocks, then the program is performed and the erase that was suspended keeps its suspend state. The program operation is allowed to be suspended (that is, nested suspend) while there is a erase suspended for a given LUN that is in the erase suspend state.

While an erase is suspended, if host issues a read command to the suspended block the read will be performed (undefined data read out) and the erase that was suspended keeps it's suspend state (SR[2] = 1). If host issues read command to block or LUN address other than the suspended block then the read is performed and the erase that was suspended keeps its suspend state (SR[2] = 1).

If the host issues an ERASE SUSPEND (61h) command while there is no erase operation ongoing the command should be ignored (that is, ^{t}ESPD = 0). If the host issues an ERASE RESUME (D2h) command while there is no erase operation ongoing or no erase suspended, the NAND will respond with a ^{t}ESPDN busy time and the LOCK status (SR[7] = 0) is set (SR[2], SR[1], and SR[0] will be "don't care"), SR[4] is reset, ESR[1] and ESR[0] will not change. If the host issues an ERASE SUSPEND (61h) to a LUN already in erase suspend state, the command will be ignored and the erase that was suspended will stay in the erase suspend state (no update of SR[2], SR[2] = 1). The host should check for previous failed operations via FAIL and FAILC status bits prior to issuing ERASE SUSPEND (61h) or ERASE RESUME (D2h).

See Restrictions During Suspend State section for Valid Operations during Erase Suspend.

Figure 112: ERASE SUSPEND (61h) Operation

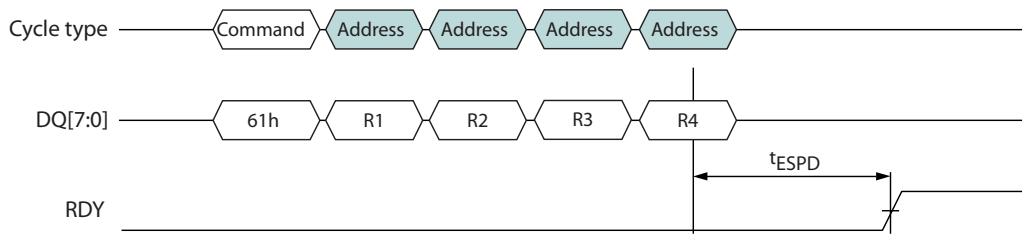
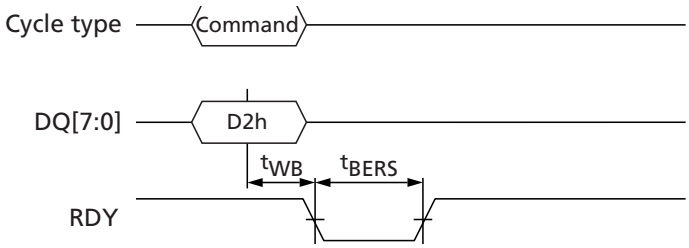


Figure 113: ERASE RESUME (D2h) Operation



Nested Suspend

Nested Suspend can be predominantly used in systems where there is a need for high performance Read IOPS.

NAND Read Operations are fastest compared to Write and Erase. Because it has the shortest life cycle, it also consumes the least resources. Nested Suspend feature is advantageous to prioritize host reads over all other operations to maximize the bandwidth as permitted by the host workload ratio.

Nested Suspend feature allows the host to suspend a program after erase is suspended. Erase suspend after program suspend is invalid. The host needs to issue PROGRAM RESUME (13h) to exit out of nested suspend state. The host needs to keep track of suspended state (erase suspend or program suspend) in a nested suspended state. Regular ERASE or ERASE RESUME (D2h) operations are not allowed until NAND exits out of nested suspend state. When using Nested Suspend, the host shall follow the specifications: ^{t}SUSPEND_P for Program Suspend and ^{t}SUSPEND_E for Erase Suspend.

While the NAND is in a nested suspend state, if the host issues a RESET (FFh, FAh, FDh) command for the affected LUN, then the suspended state is cancelled and status is cleared. The ^{t}RST time that will elapse during this operation is the maximum ^{t}RST between program and erase operations.

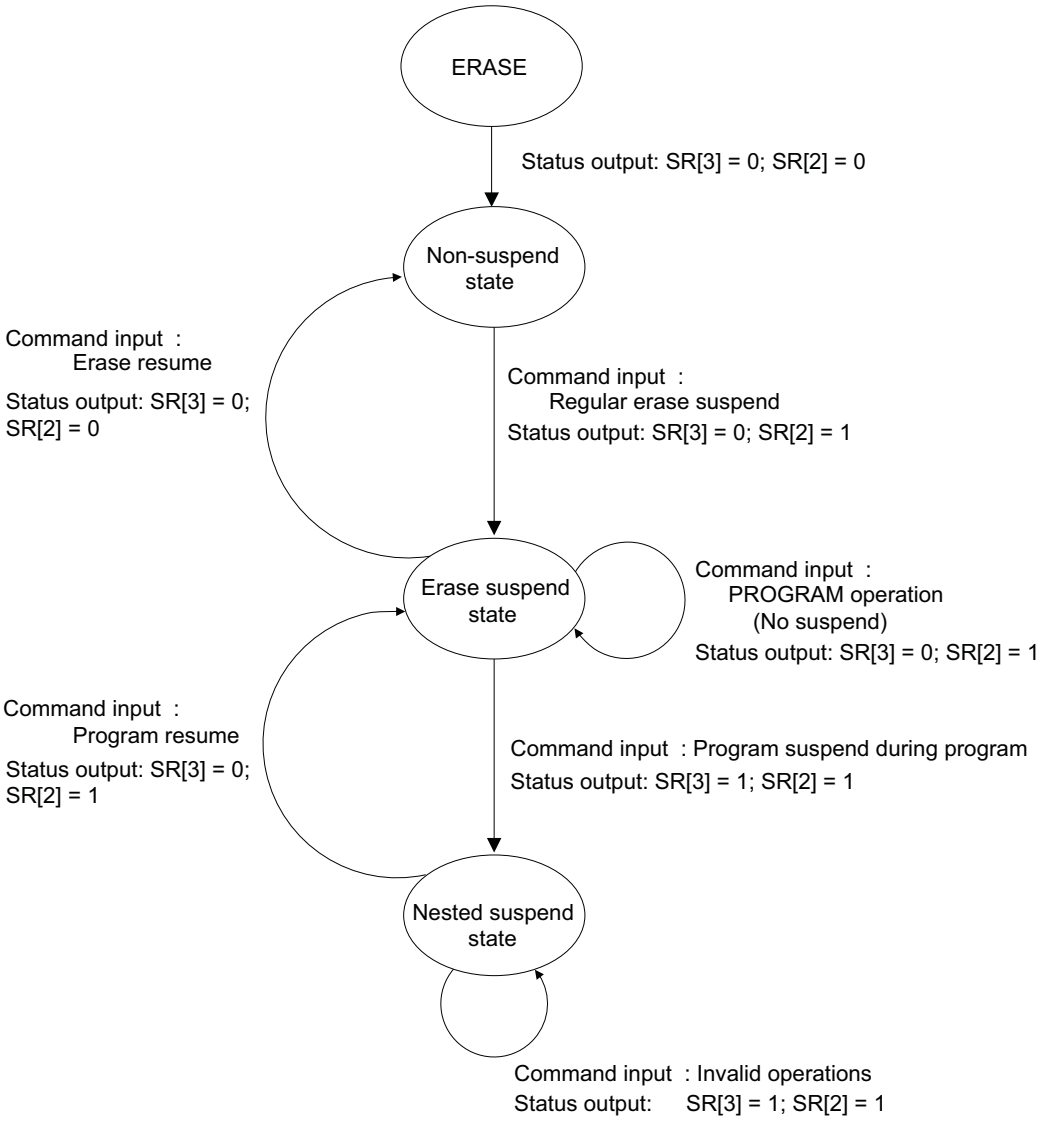
For Valid Operations during Nested Suspend, See Restrictions During Suspend State section.

SR[7], SR[3], SR[2], and SR[0] are valid after program operation is completed (ARDY=RDY = 1) until next command operation. Program Suspend SR[3] is persistent and will always reflect if a program is suspended on the LUN. SR[3] = 1 is valid after a Program Suspend [84h] command and ARDY transitions from zero to one until the suspended program is resumed or RESET (FFh, FAh, FDh) is issued. Erase Suspend SR[2] is persistent and will always reflect if an erase is suspended on the LUN. SR[2] = 1 is valid after an Erase Suspend [61h] command and ARDY transitions from zero to one until the suspended erase is resumed or RESET (FFh, FAh, FDh) is issued.

Table 74: NESTED SUSPEND Status Details

Description	SR[7] WP#	SR[3] Program Suspend	SR[2] Erase Suspend	SR[1] FailC	SR[0] Fail
Erase Suspended, Program completed with passing status (Suspend ignored)	1	0	1	X (Invalid)	0
Erase Suspended, Program completed with fail status (Suspend ignored)	1	0	1	X (Invalid)	1
Erase Suspended, Program Suspend (nested) successful	1	1	1	X (Invalid)	0
Invalid Cases: Example: Erase Resume in a Nested Suspend State	0	1	1	X (Invalid)	X (Invalid)
Invalid Cases: Example: Program Suspend or Erase Suspend in a Nested Suspend State	X (Don't Care)	1	1	X (Invalid)	X (Invalid)

Figure 114: NESTED SUSPEND Operation - State Diagram



Restrictions During Suspend State

This section lists all the allowable commands and Feature Addresses when the NAND is in a suspend state.

Table 75: Restrictions During Suspend State

Operation	Allowed During the Following Suspend Operation		
	Erase Suspend[2]	Program Suspend[2]	Nested Suspend[2]
RESET (FFh/FAh/FDh)	YES[3]	YES[3]	YES[3]
READ STATUS (70h/78h/71h/79h)	YES	YES	YES
READ PAGE (00h-30h)	YES	YES	YES
READ PAGE MULTI-PLANE (00h-32h)	YES	YES	YES
READ PAGE on Suspended Page (00h-30h/00h-32h)	NO	NO	NO
READ PAGE CACHE RANDOM (00h-31h), READ PAGE CACHE SEQUENTIAL (31h), READ PAGE CACHE MULTI-PLANE (00h-31h), READ PAGE CACHE LAST (3Fh)	YES	NO	NO
IWL READ (00h-20h)	YES	YES	YES
SBSBR - SINGLE BIT SOFT BIT READ PAGE (00h-34h)	YES	YES	YES
READ OFFSET PREFIX (2Eh)	YES	YES	YES
CHANGE READ COLUMN (05h-E0h), CHANGE READ COLUMN ENHANCED (06h-E0h/00h-05h-E0h)	YES	YES	YES
CHANGE WRITE COLUMN (85h)	YES	NO	NO
PROGRAM PAGE (80h/85h-10h), PROGRAM PAGE MULTI-PLANE (80h/85h-11h), PROGRAM PAGE CACHE (80h/85h-15h), PROGRAM PAGE CACHE MULTI-PLANE (80h/85h-15h)	YES	NO	NO
PROGRAM SUSPEND (84h)	YES	NO	NO
PROGRAM RESUME (13h)	YES	YES	YES
ERASE BLOCK (60h-D0h), ERASE BLOCK MULTI-PLANE (60h-D1h)	YES[4]	NO	NO
ERASE SUSPEND (61h)	NO	NO	NO
ERASE RESUME (D2h)	YES	NO	NO
SLC MODE LUN ENABLE (3Bh)	YES	YES	YES
VOLUME SELECT (E1h)	YES	YES	YES
SET FEATURES (EFh), GET FEATURES (EEh)	YES	YES	YES
SET FEATURES BY LUN (D4h), GET FEATURES BY LUN (D5h)	YES	YES	YES
Timing Mode (Feature Address 01h)	YES	YES	YES
NV-DDR3 Configuration (Feature Address 02h)	YES	YES	YES
Programmable Output Drive Strength (Feature Address 10h)	YES	YES	YES
Manual Dynamic Word Line Start Voltage (Feature Address 7Fh)	YES	NO	NO
Programmable RB# Pull-Down Strength (Feature Address 81h)	YES	YES	YES
Clear Extended Status Register (Feature Address 84h)	YES	YES	YES
Auto Read Calibration (Feature Address 96h)	YES	NO	NO

Table 75: Restrictions During Suspend State (Continued)

Operation	Allowed During the Following Suspend Operation		
	Erase Suspend[2]	Program Suspend[2]	Nested Suspend[2]
ACRR (Feature Address 96h)	YES	YES	YES
Read Offset Levels (Feature Addresses A0h-ABh)	YES	YES	YES
SBSBR Read Offsets (Feature Addresses E1h-E3h and B1h-B4h)	YES	YES	YES
Thermal Alert (Feature Address DAh)	YES	YES	YES
Temperature Sensor Readout (Feature Address E7h)	YES	YES	YES

Notes: 1. All other commands or Feature Addresses not listed are not allowed during any suspend operation.
2. These limitations are only valid when operation refers to the same suspended LUN.
3. Erase and Program suspend are canceled and status is cleared.
4. See ERASE SUSPEND (61h) behavior for ERASE operations Table for Erase Suspend (61h) behavior for ERASE operations.

TLC One Pass Copyback Operations

COPYBACK operations make it possible to transfer data within a plane from one page to another using the cache register. This is particularly useful for block management and wear leveling.

The COPYBACK operation is a two-step process consisting of a COPYBACK READ (00h-35h) and a COPYBACK PROGRAM (85h-10h) command. To move data from one page to another on the same plane, first issue the COPYBACK READ (00h-35h) command. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host can transfer the data to a new page by issuing the COPYBACK PROGRAM (85h-10h) command. When the die (LUN) is again ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

To prevent bit errors from accumulating over multiple COPYBACK operations, it is recommended that the host read the data out of the cache register after the COPYBACK READ (00h-35h) completes prior to issuing the COPYBACK PROGRAM (85h-10h) command. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address. The host should check the data for ECC errors and correct them. When the COPYBACK PROGRAM (85h-10h) command is issued, any corrected data can be input. The CHANGE ROW ADDRESS (85h) command can be used to change the column address.

It is not possible to use the COPYBACK operation to move data from one plane to another or from one die (LUN) to another. Instead, use a READ PAGE (00h-30h) or COPYBACK READ (00h-35h) command to read the data out of the NAND, and then use a PROGRAM PAGE (80h-10h) command with data input to program the data to a new plane or die (LUN).

Feature Address 96h: Auto Read Calibration shall not be used in conjunction with COPYBACK READ (00h-35h) or COPYBACK PROGRAM (85h-10h) operations.

Between the COPYBACK READ (00h-35h) and COPYBACK PROGRAM (85h-10h) commands, the following commands are supported: status operations (70h, 71h, 78h), and column address operations (05h-E0h, 06h-E0h, 85h). Reset operations (FFh, FAh) can be issued after COPYBACK READ (00h-35h) and the contents of the cache registers on the target or LUN are valid.

In devices which have more than one die (LUN) per target, once the COPYBACK READ (00h-35h) is issued, interleaved die (multi-LUN) operations are prohibited until after the COPYBACK PROGRAM (85h-10h) command is issued.

If a 00h command is issued to a LUN followed by address cycle input and no valid subsequent confirm command for that operation is issued (that is, 05h, 20h, 30h, 31h, 32h, 34h, 35h, and so forth), a RESET (FFh, FAh) command is required before another 00h command can be issued to that LUN to start a new read operation sequence, or to start that LUN's read operation over without executing that operation (that is, repeating or changing Address Cycle input again).

Multi-Plane Copyback Operations

Multi-plane copyback read operations improve read data throughput by copying data simultaneously from more than one plane to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the COPYBACK READ (00h-35h) command.

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command can be used to further system performance of COPYBACK PROGRAM operations by enabling movement of multiple pages from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more COPYBACK PROGRAM (85h-11h) commands in front of the COPYBACK PROGRAM (85h-10h) command. See Multi-Plane Operations for details.

COPYBACK READ (00h-35h)

The COPYBACK READ (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h. See Read Operations - READ PAGE (00h-30h) sections for further details.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the COPYBACK PROGRAM (85h-10h) command to prevent the propagation of data errors.

Figure 115: COPYBACK READ (00h-35h) Operation

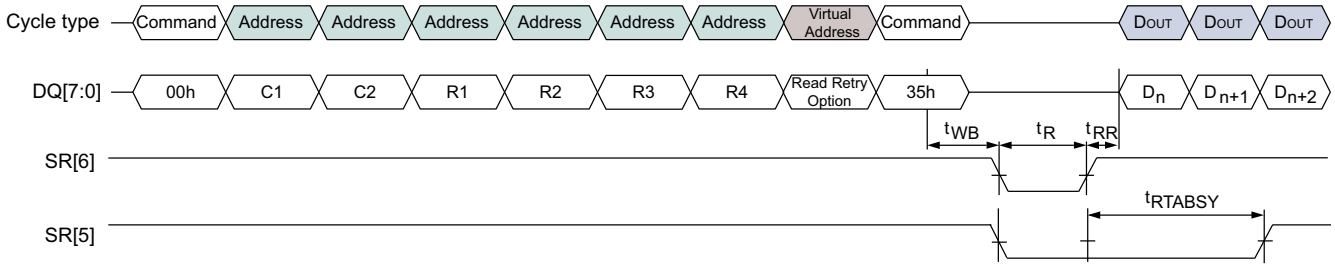
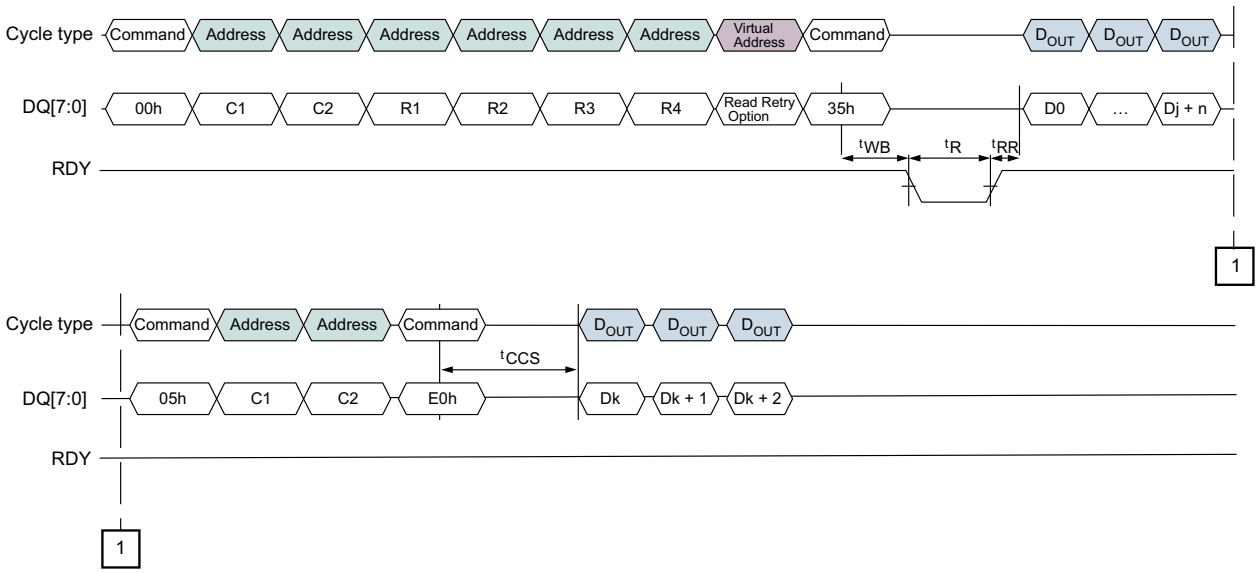


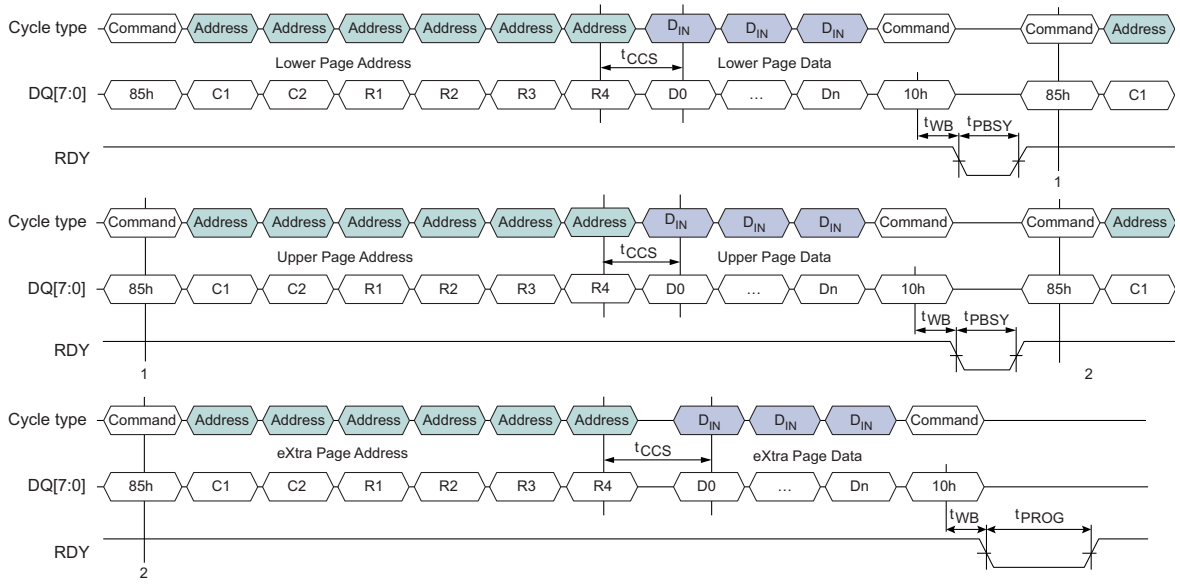
Figure 116: COPYBACK READ (00h–35h) with CHANGE READ COLUMN (05h–E0h) Operation



COPYBACK PROGRAM (85h–10h)

The COPYBACK PROGRAM (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, all cache register contents are not cleared. See PROGRAM PAGE (80h-10h) for further details.

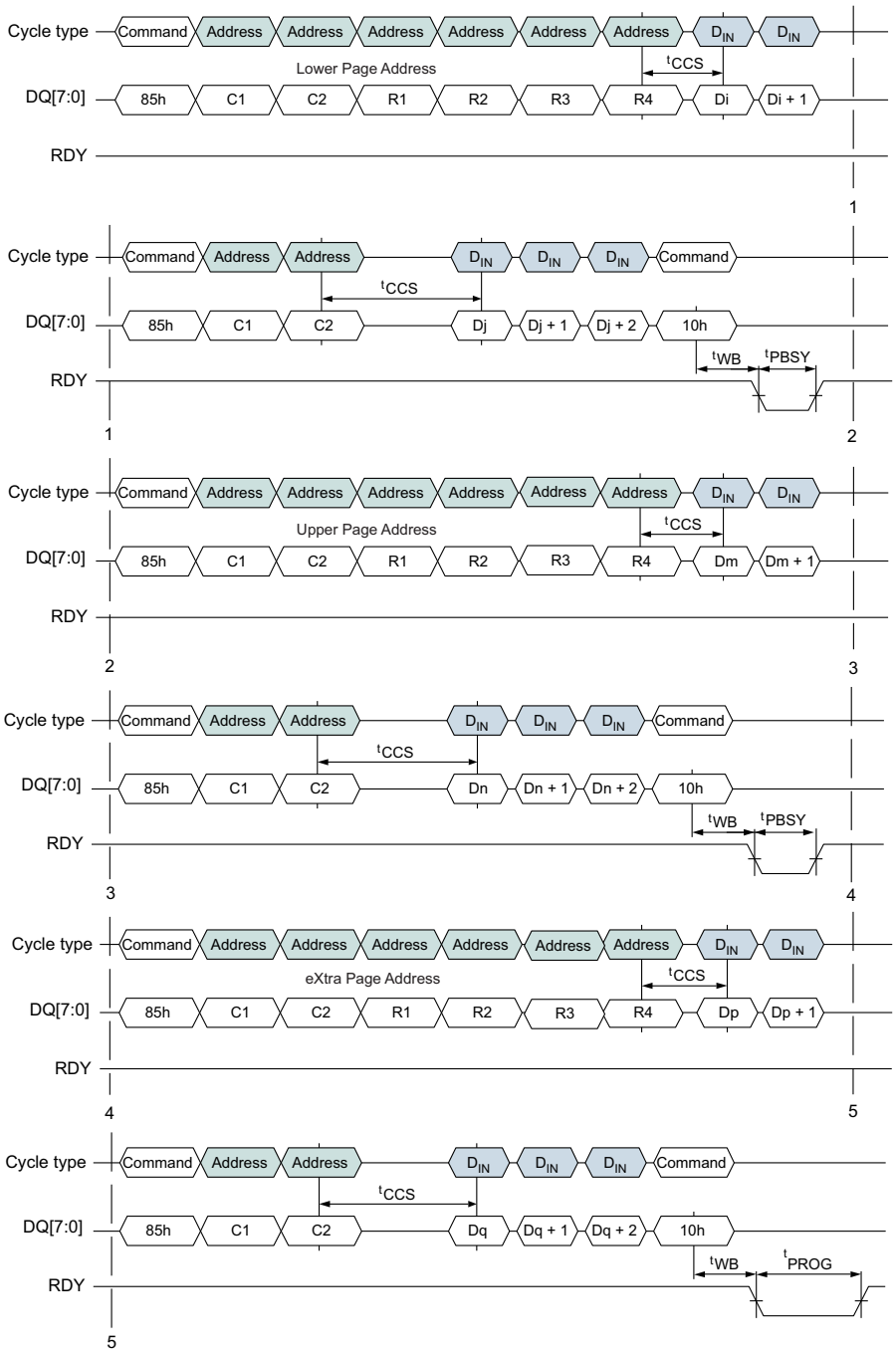
Figure 117: COPYBACK PROGRAM (85h–10h) Operation



Example command sequence for COPYBACK PROGRAM - TLC One Pass:

1. Issue COPYBACK READ (00h-35h) (It is possible for the COPYBACK READ (00h-35h) command to address a different block or page type from the subsequent 85h command, however both the 00h-35h and 85h commands must address the same plane.)
2. Read data out and identify errors (optional)
3. Issue CHANGE ROW ADDRESS (85h) + required address cycles (addressed to a lower page) to address of first error and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
4. Wait ^{t}PBSY
5. Issue COPYBACK READ (00h-35h) to another address
6. Read data out and identify errors (optional)
7. Issue CHANGE ROW ADDRESS (85h) + required address cycles (addressed to an upper page) to address of first error and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
8. Wait ^{t}PBSY
9. Issue COPYBACK READ (00h-35h) to another address
10. Read data out and identify errors (optional)
11. Issue CHANGE ROW ADDRESS (85h) + required address cycles (addressed to an eXtra page) to address of first error and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
12. Wait ^{t}PROG

Figure 118: COPYBACK PROGRAM (85h-10h) with CHANGE WRITE COLUMN (85h) Operation - TLC One Pass:



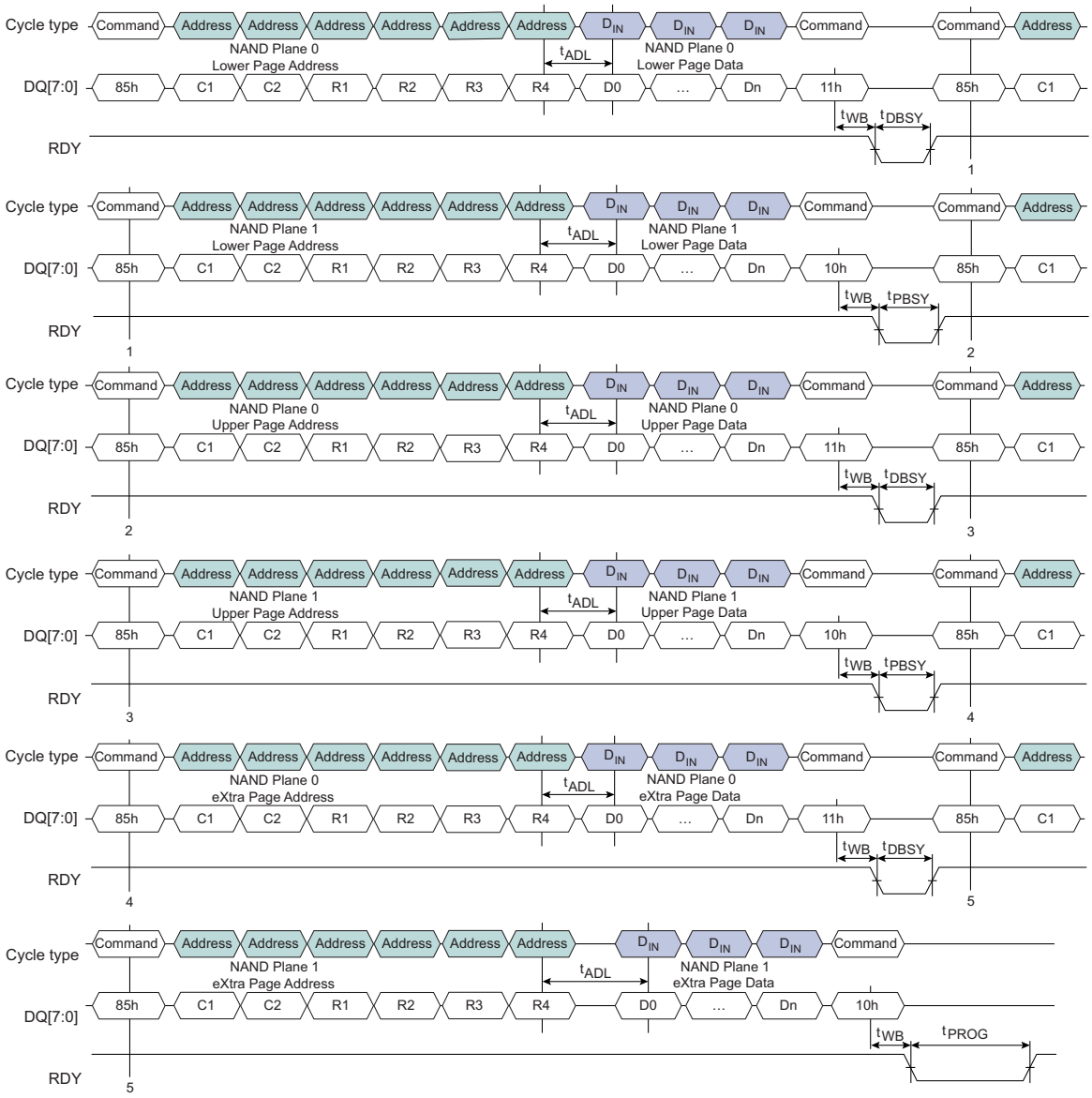
COPYBACK READ MULTI-PLANE (00h-32h)

The COPYBACK READ MULTI-PLANE (00h-32h) command is functionally identical to the READ PAGE MULTI-PLANE (00h-32h) command, except that the 35h command is written as the final command. See Read Operations - READ PAGE MULTI-PLANE (00h-32h) section for further details.

COPYBACK PROGRAM MULTI-PLANE (85h-11h)

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command is functionally identical to the PROGRAM PAGE MULTI-PLANE (80h-11h) command, except that when 85h is written to the command register, all cache register contents are not cleared. See PROGRAM PAGE MULTI-PLANE (80h-11h) for further details.

Figure 119: COPYBACK PROGRAM MULTI-PLANE (85h-11h) Operation - TLC One Pass:



Example command sequence for MULTI-PLANE COPYBACK PROGRAM - TLC One Pass (2 - Planes):

1. Issue READ PAGE MULTI-PLANE (00h-32h) to Plane 0
2. Issue COPYBACK READ (00h-35h) to Plane 1 (It is possible for the COPYBACK READ (00h-35h) commands to address a different block or page type from the subsequent 85h commands, however both the 00h-35h and 85h commands must address the same plane.)
3. Read data out for Plane 0 and identify errors (optional)

4. Issue CHANGE ROW ADDRESS (85h) + required address cycles (addressed to a lower page) to address of first error in Plane 0 and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 11h command.
5. Read out data for Plane 1 and identify errors (optional)
6. Issue CHANGE ROW ADDRESS (85h) + required address cycles (addressed to a lower page) to address of first error in Plane 1 and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
7. Wait ^{t}PBSY
8. Issue READ PAGE MULTI-PLANE (00h-32h) to the same Plane 0 address as step 1 indicated
9. Issue COPYBACK READ (00h-35h) to the same Plane 1 address as step 2 indicated
10. Read data out for Plane 0 and identify errors (optional)
11. Issue CHANGE ROW ADDRESS (85h) + required address cycles (addressed to an upper page) to address of first error in Plane 0 and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 11h command.
12. Read out data for Plane 1 and identify errors (optional)
13. Issue CHANGE ROW ADDRESS (85h) + required address cycles (addressed to an upper page) to address of first error in Plane 1 and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
14. Wait ^{t}PBSY
15. Issue READ PAGE MULTI-PLANE (00h-32h) to the same Plane 0 address as step 1 and step 8 indicated
16. Issue COPYBACK READ (00h-35h) to the same Plane 1 address as step 2 and step 9 indicated
17. Read data out for Plane 0 and identify errors (optional)
18. Issue CHANGE ROW ADDRESS (85h) + required address cycles (addressed to an eXtra page) to address of first error in Plane 0 and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 11h command.
19. Read data out for Plane 1 and identify errors (optional)
20. Issue CHANGE ROW ADDRESS (85h) + required address cycles (addressed to an eXtra page) to address of first error in Plane 1 and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
21. Wait ^{t}PROG

One-Time Programmable (OTP) Operations

This Micron NAND Flash device offers a protected, one-time programmable NAND Flash memory area. Each target has a an OTP area with a range of OTP pages (see the OTP Area Details table); the entire range is guaranteed to be good. Customers can use the OTP area in any way they desire; typical uses include programming serial numbers or other data for permanent storage.

The OTP area leaves the factory in an erased state (all bits are 1). Programming an OTP page changes bits that are 1 to 0, but cannot change bits that are 0 to 1. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area prevents further programming of the pages in the OTP area.

Enabling the OTP Operation Mode

The OTP area is accessible while the OTP operation mode is enabled. To enable OTP operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 01h to P1, followed by three cycles of 00h to P2 through P4.

When the target is in OTP operation mode, all subsequent PAGE READ (00h-30h) and PROGRAM PAGE (80h-10h) commands are applied to the OTP area.

ERASE commands are not valid while the target is in OTP operation mode.

OTP operations are not allowed during program suspend or erase suspend.

Programming OTP Pages

Each page in the OTP area is programmed using the PROGRAM OTP PAGE (80h-10h) command. Each page can only be programmed once (see NOP in the OTP Area Details table) and the host is not required to fill a page worth of data during the program command sequence. The pages in the OTP area must be programmed in ascending order.

It is illegal to issue any program command to an address outside the valid page-address range.

Protecting the OTP Area

To protect the OTP area, issue the OTP PROTECT (80h-10h) command to the OTP Protect Page. When the OTP area is protected it cannot be programmed further. It is not possible to unprotect the OTP area after it has been protected.

Reading OTP Pages

To read pages in the OTP area, whether the OTP area is protected or not, issue the PAGE READ (00h-30h) command.

If the host issues the PAGE READ (00h-30h) command to an address beyond the maximum page-address range, the data output will not be valid. To determine whether the target is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command. Use of the READ STATUS ENHANCED (78h) command or the FIXED ADDRESS READ STATUS ENHANCED (71h) command is prohibited while the OTP operation is in progress.

If a 00h command is issued to a LUN followed by address cycle input and no valid subsequent confirm command for that operation is issued (i.e. 05h, 20h, 30h, 31h, 32h, 34h, 35h, etc), a RESET (FFh, FAh) command is required before another 00h command can be issued to that LUN to start a new read operation sequence, or to start that LUN's read operation over without executing that operation (i.e. repeating or changing Address Cycle input again).

Returning to Normal Array Operation Mode

To exit OTP operation mode and return to normal array operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 00h to P1 through P4.

If the RESET (FFh, FAh) command is issued while in OTP operation mode, the target will exit OTP operation mode and enter normal operating mode.

Table 76: OTP Area Details

Description	Value
Number of OTP pages	28
OTP protect page address	01h
OTP start page address	04h
Number of partial page programs (NOP) to each OTP page	1

PROGRAM OTP PAGE (80h-10h)

The PROGRAM OTP PAGE (80h-10h) command is used to write data to the pages within the OTP area. To program data in the OTP area, the target must be in OTP operation mode.

To use the PROGRAM OTP PAGE (80h-10h) command, issue the 80h command. Issue six address cycles including the column address, the page address within the OTP page range, and a block address of 0. Next, write the data to the cache register using data input cycles. After data input is complete, issue the 10h command.

R/B# goes LOW for the duration of the array programming time, ^{t}PROG. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the READ STATUS ENHANCED (78h) command or the FIXED ADDRESS READ STATUS ENHANCED (71h) command is prohibited.

When the target is ready, read the FAIL bit of the status register to determine whether the operation passed or failed (see Status Operations).

The PROGRAM OTP PAGE (80h-10h) command also accepts the CHANGE WRITE COLUMN (85h) command during data input.

If a PROGRAM PAGE command is issued to the OTP area after the area has been protected, then R/B# goes LOW for ^{t}OBSY. After ^{t}OBSY, the status register is set to 60h.

Figure 120: PROGRAM OTP PAGE (80h-10h) Operation

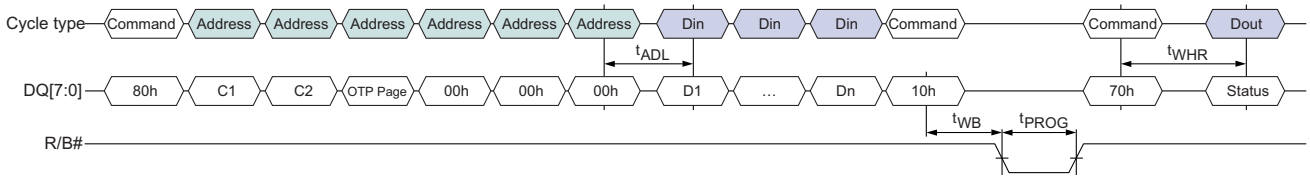
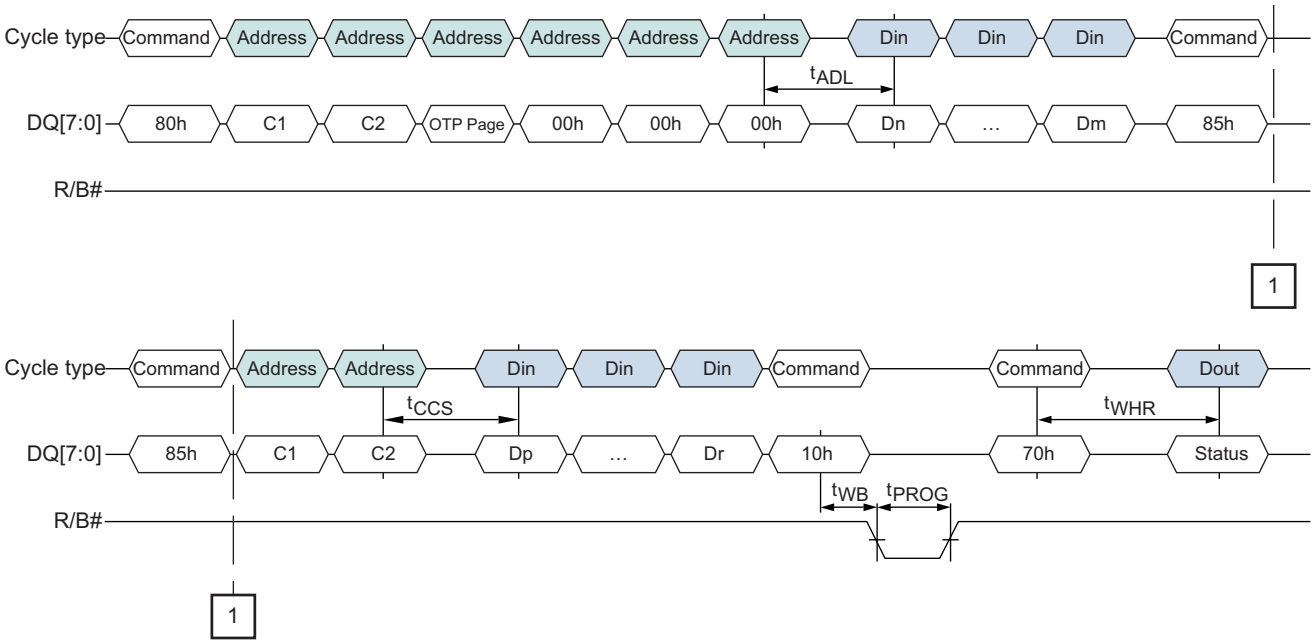


Figure 121: PROGRAM OTP PAGE (80h-10h) with CHANGE WRITE COLUMN (85h) Operation



PROTECT OTP AREA (80h-10h)

The PROTECT OTP AREA (80h-10h) command is used to prevent further programming of the pages in the OTP area. The protect the OTP area, the target must be in OTP operation mode.

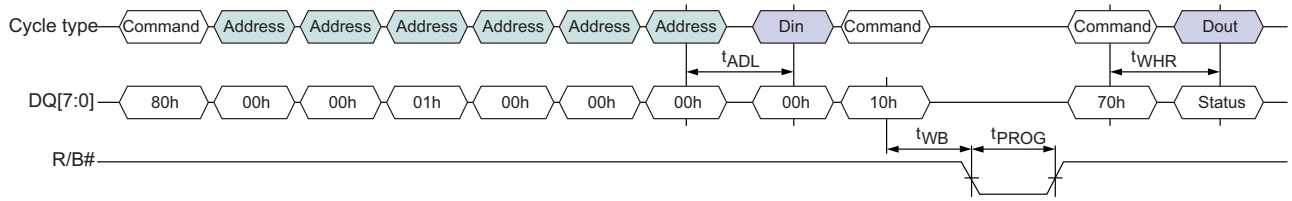
To protect all data in the OTP area, issue the 80h command. Issue six address cycles including the column address, OTP protect page address and block address; the column and block addresses are fixed to 0. Next, write 00h data for the first byte location and issue the 10h command.

R/B# goes LOW for the duration of the array programming time, ^{t}PROG. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the READ STATUS ENHANCED (78h) command or the FIXED ADDRESS READ STATUS ENHANCED (71h) command is prohibited.

When the target is ready, read the FAIL bit of the status register to determine if the operation passed or failed (see Status Operations).

If the PROTECT OTP AREA (80h-10h) command is issued after the OTP area has already been protected, R/B# goes LOW for ^{t}OBSY. After ^{t}OBSY, the status register is set to 60h.

Figure 122: PROTECT OTP AREA (80h-10h) Operation



Note: 1. OTP data is protected following a status confirmation.

READ OTP PAGE (00h-30h)

The READ OTP PAGE (00h-30h) command is used to read data from the pages in the OTP area. To read data in the OTP area, the target must be in OTP operation mode.

To use the READ OTP PAGE (00h-30h) command, issue the 00h command. Issue six address cycles including the column address, the page address within the OTP page range, and a block address of 0. Next, issue the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}R as data is transferred.

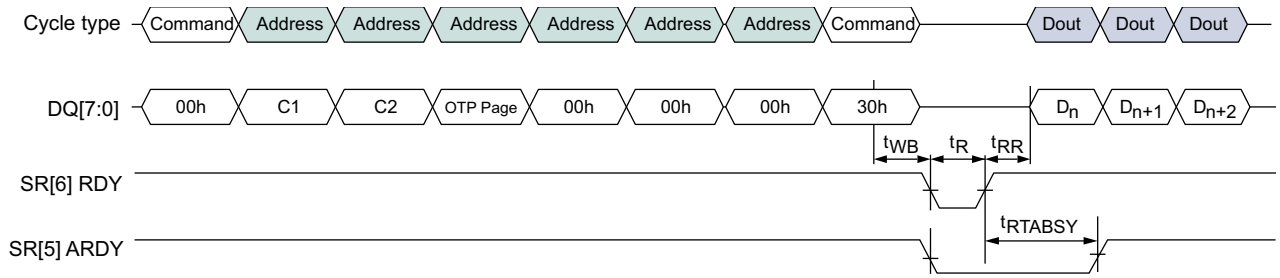
To determine the progress of the data transfer, the host can monitor the target's R/B# signal, or alternatively the READ STATUS (70h) command can be used. If the status operations are used to monitor the die's (LUN's) status, when the die (LUN) is ready (RDY = 1, ARDY = 1) the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, it begins at the column address specified.

All data from READ OTP PAGE must be output before issuing any command other than READ STATUS(70h), which requires READ MODE (00h) or CHANGE READ COLUMN (05h-E0h) command to re-enable data output. If data output is interrupted, the READ OTP PAGE (00h-30h) command needs to be reissued to the NAND.

Additional pages within the OTP area can be read by repeating the READ OTP PAGE (00h-30h) command.

The READ OTP PAGE (00h-30h) command is compatible with the CHANGE READ COLUMN (05h-E0h) command. Use of the READ STATUS ENHANCED (78h), the FIXED ADDRESS READ STATUS ENHANCED (71h), and the CHANGE READ COLUMN ENHANCED (06h-E0h) commands are prohibited.

Figure 123: READ OTP PAGE (00h-30h) Operation



Note: 1. If ACRR is enabled, the host will be required to issue a seventh address cycle.

Multi-Plane Operations

Each NAND Flash logical unit (LUN) is divided into multiple physical planes. Each plane contains a cache register and a data register independent of the other planes. The planes are addressed via the low-order block address bits. Specific details are provided in Device and Array Organization.

Multi-plane operations make better use of the NAND Flash arrays on these physical planes by performing concurrent READ, PROGRAM, or ERASE operations on multiple planes, significantly improving system performance. Multi-plane operations must be of the same type across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

When issuing MULTI-PLANE PROGRAM operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL = 1 and/or FAILC = 1), issue the READ STATUS ENHANCED (78h) command to each plane that was part of the MULTI-PLANE PROGRAM operation to determine which plane the operation failed.

When issuing MULTI-PLANE ERASE operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL = 1), issue the READ STATUS ENHANCED (78h) command to each plane that was part of the MULTI-PLANE ERASE operation to determine which plane the operation failed.

When issuing MULTI-PLANE READ operations, LUN goes busy for ^{t}R. It should be noted that when one or more blocks being read is a known factory bad block during MULTI-PLANE READ, ^{t}R busy time will be slightly longer but it is still expected to be within the maximum ^{t}R indicated on the array characteristics table.

Multi-Plane Addressing

Multi-plane commands require an address per operational plane. For a given multi-plane operation, these addresses are subject to the following requirements.

- The LUN address bit(s) must be identical for all of the issued multi-plane addresses.
- Each plane address can be issued (queued) in any order.
- Re-issuing a multi-plane program operation to the same plane is allowed prior to the program confirm command (10h/15h). However, this condition requires all addresses and data input to be identical to the previous operation to that plane.
- The page address bits, PA[11:0] for TLC and PA[9:0] for SLC, must be identical for each issued address.

The READ STATUS (70h) command should be used following MULTI-PLANE PROGRAM PAGE and ERASE BLOCK operations on a single die (LUN) target.

Interleaved Die (Multi-LUN) Operations

In devices that have more than one die (LUN) per target, it is possible to improve performance by interleaving operations between the die (LUNs). An interleaved die (multi-LUN) operation is one that individual die (LUNs) involved may be in any combination of busy or ready status during operations.

Interleaved die (multi-LUN) operations are prohibited following RESET (FFh), identification (90h, ECh, EDh), and configuration (EEh, EFh) operations until ARDY = 1 for all of the die (LUNs) on the target.

During an interleaved die (multi-LUN) operation, there are two methods to determine operation completion. The R/B# signal indicates when all of the die (LUNs) have finished their operations. R/B#

remains LOW while any die (LUN) is busy. When R/B# goes HIGH, all of the die (LUNs) are idle and the operations are complete. Alternatively, the READ STATUS ENHANCED (78h) command can report the status of each die (LUN) individually.

If a die (LUN) is performing a cache operation, like PROGRAM PAGE CACHE (80h-15h), then the die (LUN) is able to accept the data for another cache operation when status register bit 6 is 1. All operations, including cache operations, are complete on a die when status register bit 5 is 1.

Use the READ STATUS ENHANCED (78h) command to monitor status for the addressed die (LUN). When multi-plane commands are used with interleaved die (multi-LUN) operations, the multi-plane commands must also meet the requirements, see Multi-Plane Operations for details. After the READ STATUS ENHANCED (78h) command has been issued, the READ STATUS (70h) command may be issued for the previously addressed die (LUN).

See Command Definitions for the list of commands that can be issued while other die (LUNs) are busy.

During an interleaved die (multi-LUN) operation that involves a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation and a READ operation, the PROGRAM-series operation must be issued before the READ-series operation. The data from the READ-series operation must be output to the host before the next PROGRAM-series operation is issued. This is because the 80h command clears the cache register contents of all cache registers on all planes.

During a interleaved die (multi-LUN) operation that involves PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operations between multiple die (LUNs) on the same target, after data is inputted to the first die (LUN) addressed in that interleaved die (multi-LUN) sequence, before addressing the next die (LUN) with a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation a program confirm command (via 80h-10h, 80-15h) must be issued to begin the array programming of the pervious die (LUN). If this is not done by the host prior to addressing the next die (LUN), data in all the cache registers of the previously die (LUNs) will be cleared by the PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation to the next die (LUN) in the interleaved die (multi-LUN) sequence. Utilizing the Program Clear functionality in feature address 01h can be utilized to avoid a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation from clearing the contents of non-addressed NAND planes.

When issuing combinations of commands to multiple die (LUNs) (for example, Reads to one die (LUN) and Programs to another die (LUN)) or Reads to one die (LUN) and Reads to another die (LUN)), the host shall issue the READ STATUS ENHANCED (78h) command before reading data from any LUN. This ensures that only the LUN selected by the READ STATUS ENHANCED (78h) command responds to a data output cycle after being put into data output mode, and thus avoiding bus contention. After the READ STATUS ENHANCED (78h) command is issued to the selected die (LUN) a CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (00h-05h-E0h / 06h-E0h) command shall be issued prior to any data output from the selected die (LUN).

Error Management

Each NAND Flash die (LUN) is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the die (LUNs) could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per die (LUN) will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error-correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the first spare area location and the bad-block mark.

System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.

While building a bad block table, or if the host has not determined if a block is a Factory Bad Block, or thereafter when accessing a Factory Bad Block, the only commands allowed are: SLC MODE LUN ENABLE (3Bh), READ PAGE (00h-30h), READ PAGE CACHE SEQUENTIAL (31h), READ PAGE CACHE RANDOM (00h-31h), READ PAGE CACHE LAST (3Fh), and READ PAGE MULTI-PLANE (00h-32h). Read assist features from the Read Assist Feature Table are not supported when the addressed block is a Factory Bad Block.

Over time, some memory locations may fail to program or erase properly. It is not permitted to issue any PROGRAM or ERASE operation to any block that has reported a fail status via the NAND status register after a PROGRAM or ERASE operation. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation.
- Under typical conditions, use the minimum required ECC (see table below)
- Use bad-block management and wear-leveling algorithms.

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Table 77: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	2104
Total available blocks per LUN	2224
First spare area location	Byte 16,384
Bad-block mark	00h

Table 77: Error Management Details (Continued)

Description	Requirement
Minimum required ECC	TLC and SLC: LDPC to correct 1e-2 RBER for TLC and 3.25e-3 RBER for SLC/SLC pages[1]

Notes: 1. Advance ECC required to achieve specified endurance and for general array data integrity. Please contact factory for information on soft data gathering and approved list of qualified controllers.

External Data Randomization

The host needs to follow certain guidelines while performing data randomization which are listed in this section. One of the primary objectives of performing data randomization is to prevent structured data patterns from getting programmed into the NAND array. Micron does not guarantee reliability of the NAND if a structured data pattern is programmed into the NAND array. Important to note that multiple pages that are skipped or not fully programmed in terms of full page length may also constitute a structured data pattern. To avoid a structured data pattern the user must program randomized data to the entire page length (for example, all columns) even if beyond the user data.

The length of the randomizer key needs to be at least 64 bytes per 1KB sector. The SLC and MLC pages within a TLC block should follow the TLC randomization strategy.

It is recommended that each page within a block uses a unique randomization seed. In case this is not possible due to the limited seed bandwidth, the unique data should span at least 576 pages prior to repeating within the block. In addition, the repeating group boundary to boundary interface should have uniform randomness of interaction (for example, the last WL of the current group to the first WL of the next group should have equal distribution of level transition).

Seed scrambling should be done at least once before proceeding to the random data generation. This would help in preventing systematic repetition of seeds which may result in sub-optimal randomization quality.

If a page of data from one block (or multiple blocks) is copied into a new block, care must be taken to ensure that the randomization requirements are met within the destination block.

Shared Pages - TLC

In TLC NAND Flash devices, each memory cell contains multiple bits of data. These bits are distributed across NAND pages. Pages within a NAND block that share the same NAND memory cells are referred to as shared pages.

The least significant numbered shared page must be programmed before any more significant numbered shared page of those shared pages can be programmed.

Table 78: Shared Pages

Shared Pages			Shared Pages			Shared Pages			Shared Pages		
LP	UP	XP	LP	UP	XP	LP	UP	XP	LP	UP	XP
2108	–	–	2109	–	–	2110	–	–	2111	–	–
2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107
2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095
2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083
2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071
2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059
2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047
2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035
2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011
1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987
1964	1965	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975
1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963
1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951
1928	1929	1930	1931	1932	1933	1934	1935	1936	1937	1938	1939
1916	1917	1918	1919	1920	1921	1922	1923	1924	1925	1926	1927
1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915
1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
1880	1881	1882	1883	1884	1885	1886	1887	1888	1889	1890	1891
1868	1869	1870	1871	1872	1873	1874	1875	1876	1877	1878	1879
1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867
1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
1832	1833	1834	1835	1836	1837	1838	1839	1840	1841	1842	1843
1820	1821	1822	1823	1824	1825	1826	1827	1828	1829	1830	1831
1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819
1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807
1784	1785	1786	1787	1788	1789	1790	1791	1792	1793	1794	1795
1772	1773	1774	1775	1776	1777	1778	1779	1780	1781	1782	1783
1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771

Table 78: Shared Pages (Continued)

Shared Pages			Shared Pages			Shared Pages			Shared Pages		
LP	UP	XP	LP	UP	XP	LP	UP	XP	LP	UP	XP
1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
1736	1737	1738	1739	1740	1741	1742	1743	1744	1745	1746	1747
1724	1725	1726	1727	1728	1729	1730	1731	1732	1733	1734	1735
1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723
1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
1688	1689	1690	1691	1692	1693	1694	1695	1696	1697	1698	1699
1676	1677	1678	1679	1680	1681	1682	1683	1684	1685	1686	1687
1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675
1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
1640	1641	1642	1643	1644	1645	1646	1647	1648	1649	1650	1651
1628	1629	1630	1631	1632	1633	1634	1635	1636	1637	1638	1639
1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627
1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
1592	1593	1594	1595	1596	1597	1598	1599	1600	1601	1602	1603
1580	1581	1582	1583	1584	1585	1586	1587	1588	1589	1590	1591
1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579
1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
1544	1545	1546	1547	1548	1549	1550	1551	1552	1553	1554	1555
1532	1533	1534	1535	1536	1537	1538	1539	1540	1541	1542	1543
1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531
1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
1496	1497	1498	1499	1500	1501	1502	1503	1504	1505	1506	1507
1484	1485	1486	1487	1488	1489	1490	1491	1492	1493	1494	1495
1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483
1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
1448	1449	1450	1451	1452	1453	1454	1455	1456	1457	1458	1459
1436	1437	1438	1439	1440	1441	1442	1443	1444	1445	1446	1447
1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435
1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
1400	1401	1402	1403	1404	1405	1406	1407	1408	1409	1410	1411
1388	1389	1390	1391	1392	1393	1394	1395	1396	1397	1398	1399
1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387
1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
1352	1353	1354	1355	1356	1357	1358	1359	1360	1361	1362	1363
1340	1341	1342	1343	1344	1345	1346	1347	1348	1349	1350	1351
1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339

Table 78: Shared Pages (Continued)

Shared Pages			Shared Pages			Shared Pages			Shared Pages		
LP	UP	XP	LP	UP	XP	LP	UP	XP	LP	UP	XP
1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
1304	1305	1306	1307	1308	1309	1310	1311	1312	1313	1314	1315
1292	1293	1294	1295	1296	1297	1298	1299	1300	1301	1302	1303
1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291
1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
1256	1257	1258	1259	1260	1261	1262	1263	1264	1265	1266	1267
1244	1245	1246	1247	1248	1249	1250	1251	1252	1253	1254	1255
1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243
1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
1208	1209	1210	1211	1212	1213	1214	1215	1216	1217	1218	1219
1196	1197	1198	1199	1200	1201	1202	1203	1204	1205	1206	1207
1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195
1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
1160	1161	1162	1163	1164	1165	1166	1167	1168	1169	1170	1171
1148	1149	1150	1151	1152	1153	1154	1155	1156	1157	1158	1159
1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147
1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
1112	1113	1114	1115	1116	1117	1118	1119	1120	1121	1122	1123
1100	1101	1102	1103	1104	1105	1106	1107	1108	1109	1110	1111
1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099
1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
1064	1065	1066	1067	1068	1069	1070	1071	1072	1073	1074	1075
1056	1057	–	1058	1059	–	1060	1061	–	1062	1063	–
–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–
1048	1049	–	1050	1051	–	1052	1053	–	1054	1055	–
1036	1037	1038	1039	1040	1041	1042	1043	1044	1045	1046	1047
1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035
1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023
1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011
988	989	990	991	992	993	994	995	996	997	998	999
976	977	978	979	980	981	982	983	984	985	986	987
964	965	966	967	968	969	970	971	972	973	974	975
952	953	954	955	956	957	958	959	960	961	962	963
940	941	942	943	944	945	946	947	948	949	950	951
928	929	930	931	932	933	934	935	936	937	938	939

Table 78: Shared Pages (Continued)

Shared Pages			Shared Pages			Shared Pages			Shared Pages		
LP	UP	XP	LP	UP	XP	LP	UP	XP	LP	UP	XP
916	917	918	919	920	921	922	923	924	925	926	927
904	905	906	907	908	909	910	911	912	913	914	915
892	893	894	895	896	897	898	899	900	901	902	903
880	881	882	883	884	885	886	887	888	889	890	891
868	869	870	871	872	873	874	875	876	877	878	879
856	857	858	859	860	861	862	863	864	865	866	867
844	845	846	847	848	849	850	851	852	853	854	855
832	833	834	835	836	837	838	839	840	841	842	843
820	821	822	823	824	825	826	827	828	829	830	831
808	809	810	811	812	813	814	815	816	817	818	819
796	797	798	799	800	801	802	803	804	805	806	807
784	785	786	787	788	789	790	791	792	793	794	795
772	773	774	775	776	777	778	779	780	781	782	783
760	761	762	763	764	765	766	767	768	769	770	771
748	749	750	751	752	753	754	755	756	757	758	759
736	737	738	739	740	741	742	743	744	745	746	747
724	725	726	727	728	729	730	731	732	733	734	735
712	713	714	715	716	717	718	719	720	721	722	723
700	701	702	703	704	705	706	707	708	709	710	711
688	689	690	691	692	693	694	695	696	697	698	699
676	677	678	679	680	681	682	683	684	685	686	687
664	665	666	667	668	669	670	671	672	673	674	675
652	653	654	655	656	657	658	659	660	661	662	663
640	641	642	643	644	645	646	647	648	649	650	651
628	629	630	631	632	633	634	635	636	637	638	639
616	617	618	619	620	621	622	623	624	625	626	627
604	605	606	607	608	609	610	611	612	613	614	615
592	593	594	595	596	597	598	599	600	601	602	603
580	581	582	583	584	585	586	587	588	589	590	591
568	569	570	571	572	573	574	575	576	577	578	579
556	557	558	559	560	561	562	563	564	565	566	567
544	545	546	547	548	549	550	551	552	553	554	555
532	533	534	535	536	537	538	539	540	541	542	543
520	521	522	523	524	525	526	527	528	529	530	531
508	509	510	511	512	513	514	515	516	517	518	519
496	497	498	499	500	501	502	503	504	505	506	507

Table 78: Shared Pages (Continued)

Shared Pages			Shared Pages			Shared Pages			Shared Pages		
LP	UP	XP	LP	UP	XP	LP	UP	XP	LP	UP	XP
484	485	486	487	488	489	490	491	492	493	494	495
472	473	474	475	476	477	478	479	480	481	482	483
460	461	462	463	464	465	466	467	468	469	470	471
448	449	450	451	452	453	454	455	456	457	458	459
436	437	438	439	440	441	442	443	444	445	446	447
424	425	426	427	428	429	430	431	432	433	434	435
412	413	414	415	416	417	418	419	420	421	422	423
400	401	402	403	404	405	406	407	408	409	410	411
388	389	390	391	392	393	394	395	396	397	398	399
376	377	378	379	380	381	382	383	384	385	386	387
364	365	366	367	368	369	370	371	372	373	374	375
352	353	354	355	356	357	358	359	360	361	362	363
340	341	342	343	344	345	346	347	348	349	350	351
328	329	330	331	332	333	334	335	336	337	338	339
316	317	318	319	320	321	322	323	324	325	326	327
304	305	306	307	308	309	310	311	312	313	314	315
292	293	294	295	296	297	298	299	300	301	302	303
280	281	282	283	284	285	286	287	288	289	290	291
268	269	270	271	272	273	274	275	276	277	278	279
256	257	258	259	260	261	262	263	264	265	266	267
244	245	246	247	248	249	250	251	252	253	254	255
232	233	234	235	236	237	238	239	240	241	242	243
220	221	222	223	224	225	226	227	228	229	230	231
208	209	210	211	212	213	214	215	216	217	218	219
196	197	198	199	200	201	202	203	204	205	206	207
184	185	186	187	188	189	190	191	192	193	194	195
172	173	174	175	176	177	178	179	180	181	182	183
160	161	162	163	164	165	166	167	168	169	170	171
148	149	150	151	152	153	154	155	156	157	158	159
136	137	138	139	140	141	142	143	144	145	146	147
124	125	126	127	128	129	130	131	132	133	134	135
112	113	114	115	116	117	118	119	120	121	122	123
100	101	102	103	104	105	106	107	108	109	110	111
88	89	90	91	92	93	94	95	96	97	98	99
76	77	78	79	80	81	82	83	84	85	86	87
64	65	66	67	68	69	70	71	72	73	74	75

Table 78: Shared Pages (Continued)

Shared Pages			Shared Pages			Shared Pages			Shared Pages		
LP	UP	XP	LP	UP	XP	LP	UP	XP	LP	UP	XP
52	53	54	55	56	57	58	59	60	61	62	63
40	41	42	43	44	45	46	47	48	49	50	51
28	29	30	31	32	33	34	35	36	37	38	39
16	17	18	19	20	21	22	23	24	25	26	27
4	5	6	7	8	9	10	11	12	13	14	15
0	–	–	1	–	–	2	–	–	3	–	–

Output Drive Impedance (NV-DDR3)

For the NV-DDR3 interface, the two supported settings for output driver strength are: 37.5 ohms and 50 ohms. The 37.5 ohm output drive strength setting is the power-on default value.

The drive strength setting should be selected based on the signal integrity requirements of the channel. The host can change the output drive strength setting using the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command.

The output impedance range from minimum to maximum covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal line.

Table 79: Output Drive Strength Conditions (V_{CCQ} = 1.14–1.26V)

Range	Process	Voltage	Temperature
Minimum	Slow-Slow	1.14V	T_{OPER} (MAX)
Nominal	Typical-Typical	1.2V	+25°C
Maximum	Fast-Fast	1.26V	T_{OPER} (MIN)

Table 80: Output Drive Strength Impedance Values Without ZQ Calibration (V_{CCQ} = 1.14–1.26V)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
37.5 ohms	Rpd	V_{CCQ} × 0.2	17.1	37.5	65.5	ohms
		V_{CCQ} × 0.5	22.5	37.5	65.5	ohms
		V_{CCQ} × 0.8	22.5	37.5	91.4	ohms
	Rpu	V_{CCQ} × 0.2	22.5	37.5	91.4	ohms
		V_{CCQ} × 0.5	22.5	37.5	65.5	ohms
		V_{CCQ} × 0.8	17.1	37.5	65.5	ohms

Table 80: Output Drive Strength Impedance Values Without ZQ Calibration (V_{CCQ} = 1.14–1.26V)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
50 ohms	Rpd	V_{CCQ} × 0.2	24.0	50.0	87.0	ohms
		V_{CCQ} × 0.5	30.0	50.0	87.0	ohms
		V_{CCQ} × 0.8	30.0	50.0	122.0	ohms
	Rpu	V_{CCQ} × 0.2	30.0	50.0	122.0	ohms
		V_{CCQ} × 0.5	30.0	50.0	87.0	ohms
		V_{CCQ} × 0.8	24.0	50.0	87.0	ohms

Table 81: Output Drive Strength Impedance Values With ZQ Calibration (V_{CCQ} = 1.14–1.26V)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
37.5 ohms	Rpd	V_{CCQ} × 0.2	0.57	1	1.15	$R_{ZQ}/8$
		V_{CCQ} × 0.5	0.85	1	1.15	$R_{ZQ}/8$
		V_{CCQ} × 0.8	0.85	1	1.47	$R_{ZQ}/8$
	Rpu	V_{CCQ} × 0.2	0.85	1	1.47	$R_{ZQ}/8$
		V_{CCQ} × 0.5	0.85	1	1.15	$R_{ZQ}/8$
		V_{CCQ} × 0.8	0.57	1	1.15	$R_{ZQ}/8$
50 ohms	Rpd	V_{CCQ} × 0.2	0.57	1	1.15	$R_{ZQ}/6$
		V_{CCQ} × 0.5	0.85	1	1.15	$R_{ZQ}/6$
		V_{CCQ} × 0.8	0.85	1	1.47	$R_{ZQ}/6$
	Rpu	V_{CCQ} × 0.2	0.85	1	1.47	$R_{ZQ}/6$
		V_{CCQ} × 0.5	0.85	1	1.15	$R_{ZQ}/6$
		V_{CCQ} × 0.8	0.57	1	1.15	$R_{ZQ}/6$

Notes: 1. Tolerance limits assume R_{ZQ} of 300 ohms ±1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.

If either the temperature or the voltage changes after the ZQ calibration operation, then output drive strength impedance tolerance limits can be expected to widen according to Output Drive Sensitivity

With ZQ Calibration Table and Output Driver Voltage and Temperature Sensitivity With ZQ Calibration Table .

Table 82: Output Drive Sensitivity With ZQ Calibration

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Maximum	Unit
37.5 ohms	Rpd	V_{CCQ} × 0.2	0.57 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/8$
		V_{CCQ} × 0.5	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/8$
		V_{CCQ} × 0.8	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.47 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/8$
	Rpu	V_{CCQ} × 0.2	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.47 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/8$
		V_{CCQ} × 0.5	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/8$
		V_{CCQ} × 0.8	0.57 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/8$
50 ohms	Rpd	V_{CCQ} × 0.2	0.57 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/6$
		V_{CCQ} × 0.5	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/6$
		V_{CCQ} × 0.8	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.47 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/6$
	Rpu	V_{CCQ} × 0.2	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ?V	1.47 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/6$
		V_{CCQ} × 0.5	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/6$
		V_{CCQ} × 0.8	0.57 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/6$

Table 83: Output Driver Voltage and Temperature Sensitivity With ZQ Calibration

Chnage	Minimum	Maximum	Unit
$dR_{ON}dT$	0	0.5	%/°C
$dR_{ON}dV$	0	0.2	%/mV

Table 84: Pull-Up and Pull-Down Output Impedance Mismatch Without ZQ Calibration for NV-DDR3

Drive Strength	Minimum	Maximum	Unit	Notes
37.5 ohms	0	6.64	ohms	1, 2
50 ohms	0	8.8	ohms	1, 2

Notes: 1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.

2. Test conditions: $V_{CCQ} = V_{CCQ}$ (MIN), $V_{OUT} = V_{CCQ} \times 0.5$, T_{OPER}.

Table 85: Pull-Up and Pull-Down Output Impedance Mismatch With ZQ Calibration for NV-DDR3

Drive Strength	Minimum	Maximum	Unit	Notes
37.5 ohms	0	5.62	ohms	1, 2
50 ohms	0	7.5	ohms	1, 2

Notes: 1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2. Test conditions: $V_{CCQ} = V_{CCQ}$ (MIN), $V_{OUT} = V_{CCQ} \times 0.5$, T_{OPER}.

AC Overshoot/Undershoot Specifications

The supported AC overshoot and undershoot area depends on the timing mode selected by the host. NAND devices may have different maximum amplitude requirements for overshoot and undershoot than the host controller. If the host controller has more stringent requirements, termination or other means of reducing overshoot or undershoot may be required beyond the NAND requirements.

Table 86: NV-DDR3 Overshoot/Undershoot Parameters For Timing Modes 0–12

Parameter	Signals	Timing Mode													Unit
		0	1	2	3	4	5	6	7	8	9	10	11	12	
Maximum peak amplitude provided for overshoot area	–	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	V
Maximum peak amplitude provided for undershoot area	–	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	V
Maximum overshoot area above V_{CCQ}	DQ[7:0], DQS, RE#	2	2	1.2	0.96	0.8	0.6	0.48	0.4	0.3	0.24	0.2	0.15	0.13	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	3	3	3	3	3	
Maximum undershoot area below V_{SSQ}	DQ[7:0], DQS, RE#	2	2	1.2	0.96	0.8	0.6	0.48	0.4	0.3	0.24	0.2	0.15	0.13	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	3	3	3	3	3	

Table 87: NV-DDR3 Overshoot/Undershoot Parameters For Timing Modes 13–15

Parameter	Signals	Timing Mode			Unit
		13	14	15	
Maximum peak amplitude provided for overshoot area	–	0.35	0.35	0.35	V
Maximum peak amplitude provided for undershoot area	–	0.35	0.35	0.35	V
Maximum overshoot area above V_{CCQ}	DQ[7:0], DQS, RE#	0.12	0.11	0.10	V-ns
	ALE, CLE, WE#	3	3	3	
Maximum undershoot area below V_{SSQ}	DQ[7:0], DQS, RE#	0.12	0.11	0.10	V-ns
	ALE, CLE, WE#	3	3	3	

Figure 124: Overshoot

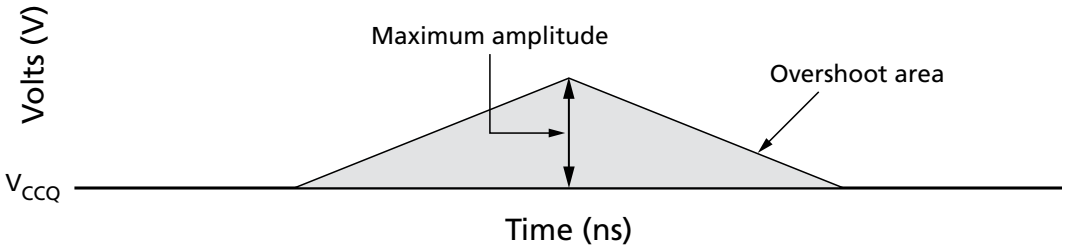
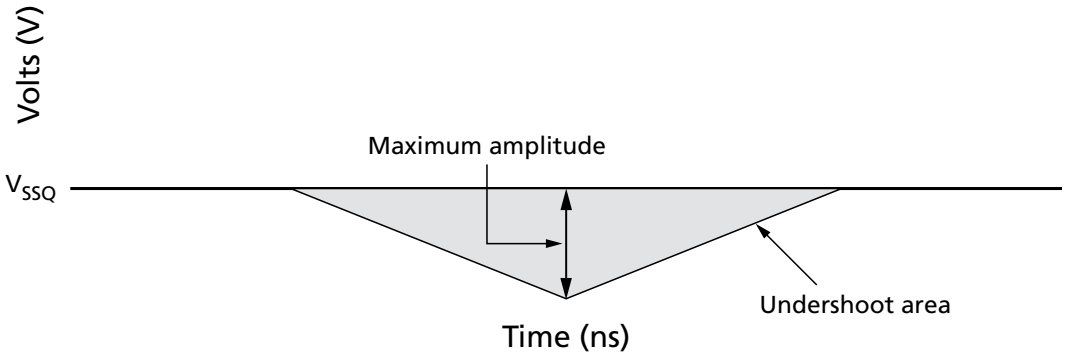


Figure 125: Undershoot



Input Slew Rate

Though all AC timing parameters are tested with a nominal input slew rate of 1 V/ns, it is possible to run the device at a slower slew rate. The input slew rates shown below are sampled, and not 100% tested. When using slew rates slower than the minimum values, timing must be derated by the host.

Table 88: Test Conditions for Input Slew Rate

Parameter	Value
Rising edge for setups	The last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IH(AC)}$ min
Falling edge for setups	The last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IL(AC)}$ max
Rising edge for holds	The first crossing of $V_{IL(DC)}$ max and the first crossing of $V_{REFQ(DC)}$
Falling edge for holds	The first crossing of $V_{IH(DC)}$ min and the first crossing of $V_{REFQ(DC)}$
Temperature range	T_A

The minimum and maximum input slew rate requirements that the device shall comply with below for NV-DDR3 operations. If the input slew rate falls below the minimum value, then derating shall be applied.

Table 89: Maximum and Minimum Input Slew Rate

Description	Single Ended	Differential	Unit
Input slew rate (min)	1.0	2.0[1]	V/ns
Input slew rate (max)	4.5	9.0[1]	V/ns

Notes: 1. Input differential slew rates are measured between $V_{IL(DC)}$ and $V_{IH(DC)}$. Signals must be linear between these thresholds.

For DQ signals when used for input, the total data setup time (^{t}DS) and data hold time (^{t}DH) required is calculated by adding a derating value to the ^{t}DS and ^{t}DH values indicated for the timing mode. To calculate the total data setup time, ^{t}DS is incremented by the appropriate Δset derating value. To calculate the total data hold time, ^{t}DH is incremented by the appropriate Δhold derating value. The Input Slew Rate Derating for NV-DDR3 Single-Ended (V_{CCQ} = 1.14–1.26V) - ps Units table provides the derating values when single-ended DQS is used. The Input Slew Rate Derating for NV-DDR3 Differential (V_{CCQ} = 1.14–1.26V) - ps Units table provides the derating values when differential DQS (DQS_t/DQS_c) is used.

The setup nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IH(AC)}$ min. The setup nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IL(AC)}$ max. If the actual signal is always earlier than the nominal slew rate line between the shaded '$V_{REFQ(DC)}$ to AC region', then the derating value uses the nominal slew rate shown in Figure 126. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REFQ(DC)}$ to AC region', then the derating value uses the slew rate of a tangent line to the actual signal from the AC level to the DC level shown in Figure 127.

The hold nominal slew rate for a rising signal is defined as the slew rate between the first crossing of $V_{IL(DC)}$ max and the first crossing of $V_{REFQ(DC)}$. The hold nominal slew rate for a falling signal is defined as the slew rate between the first crossing of $V_{IH(DC)}$ min and the first crossing of $V_{REFQ(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded 'DC to $V_{REFQ(DC)}$ region', then the

derating value uses the nominal slew rate shown in Figure 128. If the actual signal is earlier than the nominal slew rate line anywhere between the shaded 'DC to $V_{REFQ(DC)}$ region', then the derating value uses the slew rate of a tangent line to the actual signal from the DC level to the $V_{REFQ(DC)}$ level shown in Figure 129.

If the tangent line is used for derating, the setup and hold values shall be derated from where the tangent line crosses $V_{REFQ(DC)}$, not the actual signal (refer to Figure 127 and Figure 129).

For slew rates not explicitly listed in the Input Slew Rate Derating for NV-DDR3 Single-Ended (V_{CCQ} = 1.14–1.26V) - ps Units and Input Slew Rate Derating for NV-DDR3 Differential (V_{CCQ} = 1.14–1.26V) - ps Units tables, the derating values should be obtained by linear interpolation. These values are typically not subject to production test; the values are verified by design and characterization.

Table 90: Input Slew Rate Derating for NV-DDR3 Single-Ended (V_{CCQ} = 1.14–1.26V) - ps Units

DQ V/ns	Δ^tDS, Δ^tDH Derating (ps) $V_{IH(AC)}/V_{IL(AC)} = V_{REF} \pm 150mV$, $V_{IH(DC)}/V_{IL(DC)} = V_{REF} \pm 100mV$									
	DQS Slew Rate									
	2	1.5	1	0.9	0.8	0.7	0.6	0.5	0.4	0.3
	Set / Hold	Set / Hold	Set / Hold	Set / Hold	Set / Hold	Set / Hold	Set / Hold	Set / Hold	Set / Hold	Set / Hold
2	0 / 0	0 / 0	0 / 0	–	–	–	–	–	–	–
1.5	0 / 0	0 / 0	0 / 0	11 / 0	–	–	–	–	–	–
1	0 / 0	0 / 0	0 / 0	11 / 0	25 / 0	–	–	–	–	–
0.9	–	0 / 0	11 / 0	22 / 0	36 / 0	54 / 0	–	–	–	–
0.8	–	–	25 / 0	39 / 0	50 / 0	68 / 0	92 / 0	–	–	–
0.7	–	–	–	54 / 0	68 / 0	86 / 0	110 / 0	143 / 0	–	–
0.6	–	–	–	–	92 / 0	110 / 0	133 / 0	167 / 0	217 / 0	–
0.5	–	–	–	–	–	143 / 0	167 / 0	200 / 0	250 / 0	333 / 0
0.4	–	–	–	–	–	–	217 / 0	250 / 0	300 / 0	383 / 0
0.3	–	–	–	–	–	–	–	333 / 0	383 / 0	467 / 0

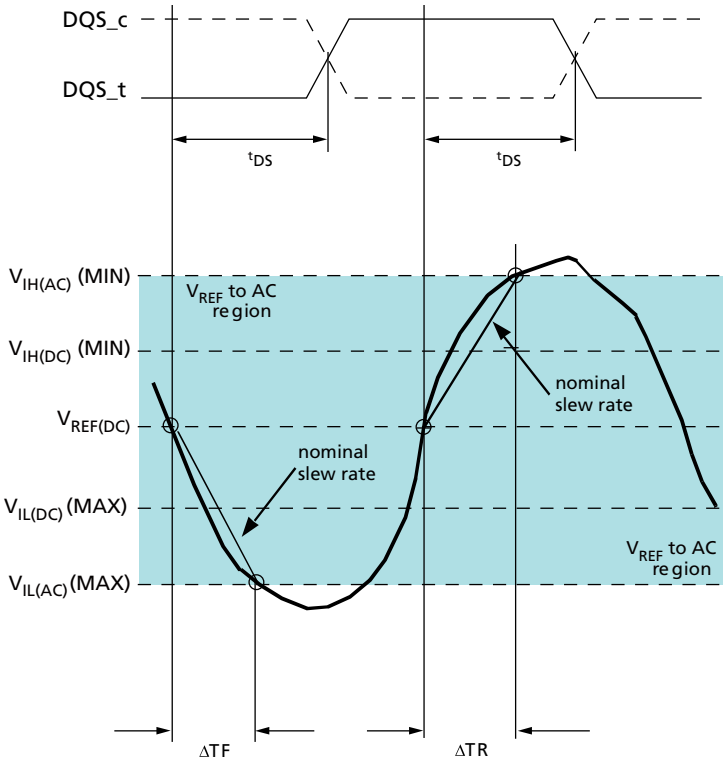
Table 91: Input Slew Rate Derating for NV-DDR3 Differential (V_{CCQ} = 1.14–1.26V) - ps Units

DQ V/ns	Δ^tDS, Δ^tDH Derating (ps) $V_{IH(AC)}/V_{IL(AC)} = V_{REF} \pm 150mV$, $V_{IH(DC)}/V_{IL(DC)} = V_{REF} \pm 100mV$															
	DQS_t/DQS_c Slew Rate															
	2		1.8		1.6		1.4		1.2		1		0.8		0.6	
	Set	Hold	Set	Hold	Set	Hold	Set	Hold	Set	Hold	Set	Hold	Set	Hold	Set	Hold
2	0	0	–	–	–	–	–	–	–	–	–	–	–	–	–	–
1.5	0	0	6	6	–	–	–	–	–	–	–	–	–	–	–	–
1	0	0	6	6	13	13	–	–	–	–	–	–	–	–	–	–
0.9	11	11	17	17	24	24	33	33	–	–	–	–	–	–	–	–
0.8	25	25	31	31	38	38	46	46	58	58	–	–	–	–	–	–
0.7	–	–	48	48	55	55	64	64	75	75	75	75	–	–	–	–
0.6	–	–	–	–	79	79	88	88	100	100	100	100	100	100	–	–

Table 91: Input Slew Rate Derating for NV-DDR3 Differential (V_{CCQ} = 1.14–1.26V) - ps Units

DQ V/ns	Δ^tDS, Δ^tDH Derating (ps) $V_{IH(AC)}/V_{IL(AC)} = V_{REF} \pm 150mV$, $V_{IH(DC)}/V_{IL(DC)} = V_{REF} \pm 100mV$															
	DQS_t/DQS_c Slew Rate															
	2		1.8		1.6		1.4		1.2		1		0.8		0.6	
	Set	Hold	Set	Hold	Set	Hold	Set	Hold	Set	Hold	Set	Hold	Set	Hold	Set	Hold
0.5	–	–	–	–	–	–	121	121	125	125	125	125	125	125	125	125
0.4	–	–	–	–	–	–	–	–	150	150	150	150	150	150	150	150
0.3	–	–	–	–	–	–	–	–	–	–	175	175	175	175	175	175

Figure 126: Nominal Slew Rate for Data Setup Time (^tDS)



$$\text{Setup slew rate falling signal} = \frac{V_{REF(DC)} - V_{IL(AC)}(MAX)}{\Delta TF} \qquad \text{Setup slew rate rising signal} = \frac{V_{IH(AC)}(MIN) - V_{REF(DC)}}{\Delta TR}$$

Illustration of nominal slew rate for setup time ^tDS

Figure 127: Tangent Line for Data Setup Time (^{t}DS)

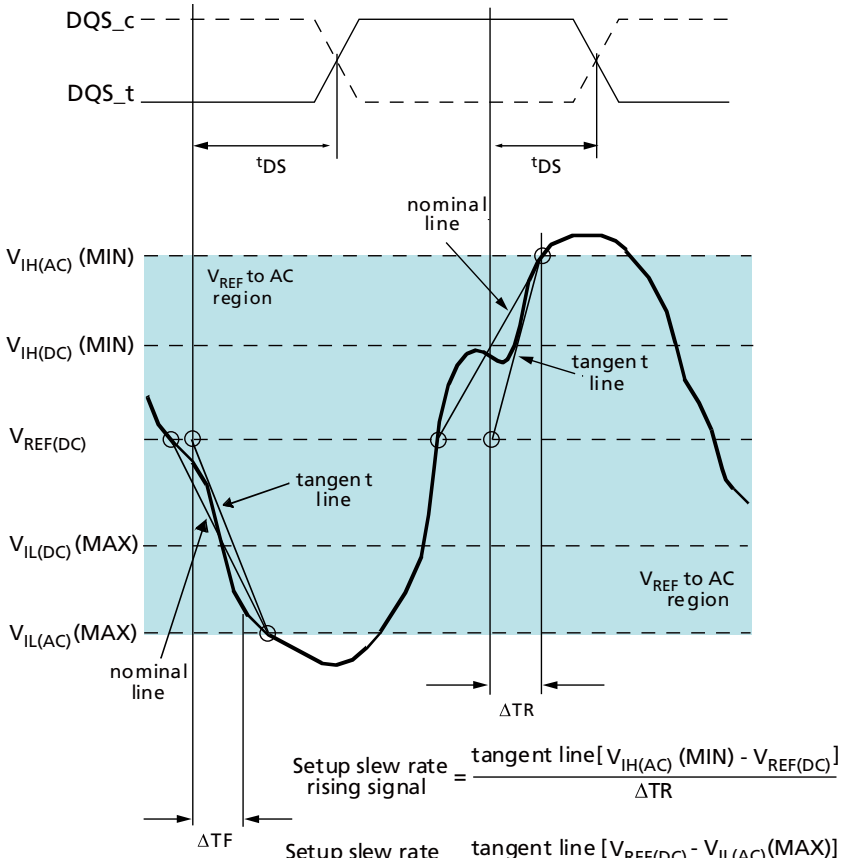
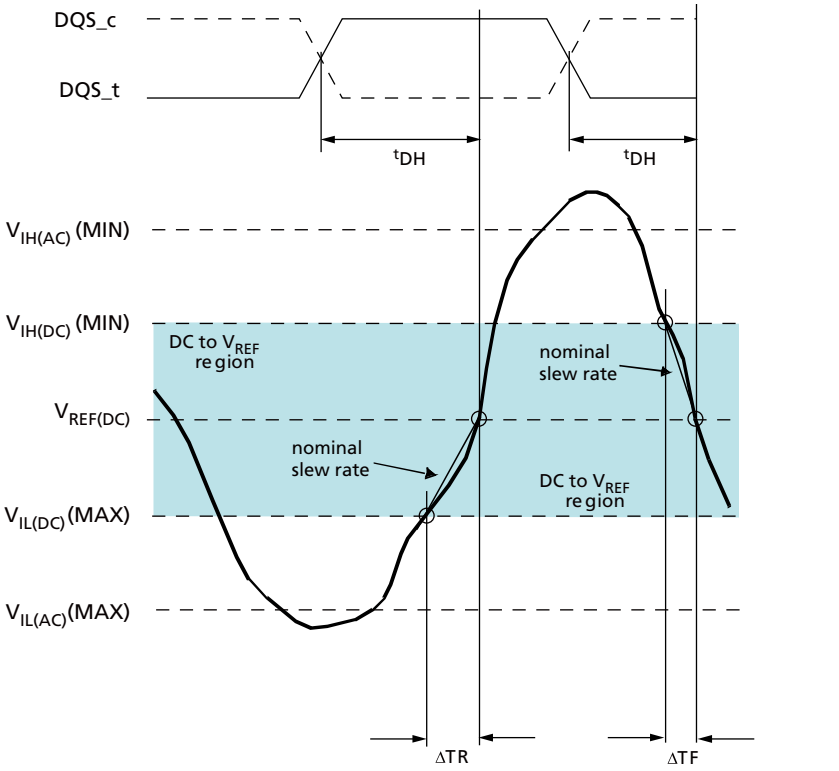


Illustration of tangent line for setup time ^{t}DS

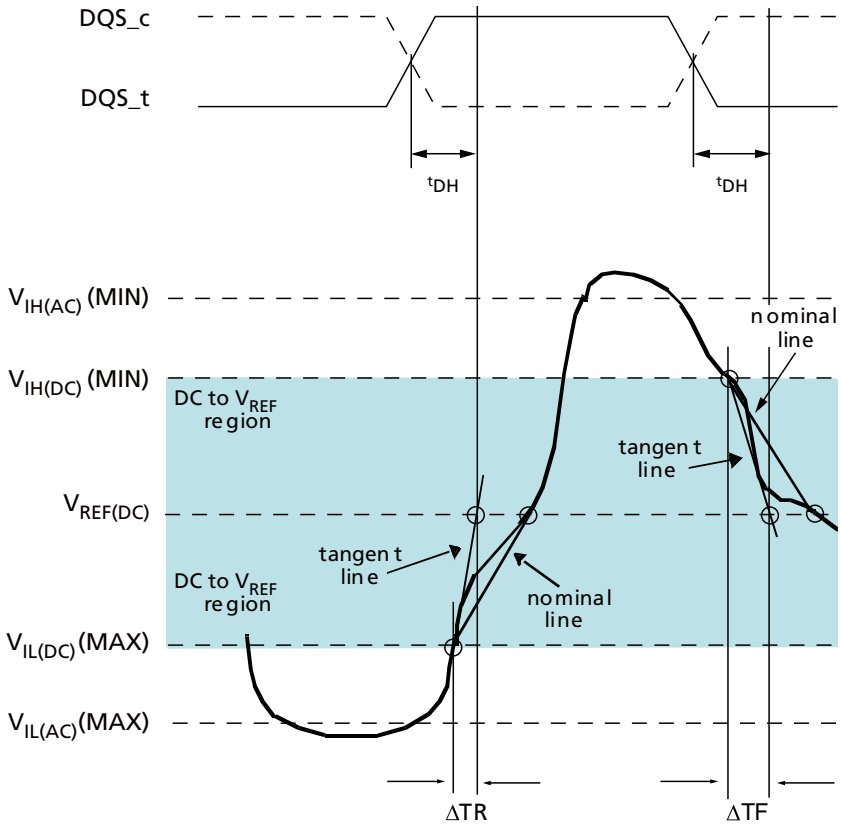
Figure 128: Nominal Slew Rate for Data Hold Time (^{t}DH)



$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)}(MAX)}{\Delta TR} \qquad \text{Hold slew rate falling signal} = \frac{V_{IH(DC)}(MIN) - V_{REF(DC)}}{\Delta TF}$$

Illustration of nominal slew rate for hold time ^{t}DH

Figure 129: Tangent Line for Data Hold Time (^{t}DH)



$$\text{Hold slew rate rising signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)}(MAX)]}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{tangent line } [V_{IH(DC)}(MIN) - V_{REF(DC)}]}{\Delta TF}$$

Illustration of tangent line for for hold time ^{t}DH

Output Slew Rate

The output slew rate is tested using the following setup with only one die per DQ channel.

Table 92: Test Conditions for Output Slew Rate

Parameter	NV-DDR3 Single-Ended	NV-DDR3 Differential
$V_{OL(DC)}$	–	–
$V_{OH(DC)}$	–	–
$V_{OL(AC)}$[1]	V_{TT} - (V_{CCQ} × 0.10)	–
$V_{OH(AC)}$[1]	V_{TT} + (V_{CCQ} × 0.10)	–
$V_{OLdiff(AC)}$	–	0.2 × V_{CCQ}
$V_{OHdiff(AC)}$	–	0.2 × V_{CCQ}
Rising edge (^{t}RISE)	$V_{OL(AC)}$ to $V_{OH(AC)}$	–
Falling edge (^{t}FALL)	$V_{OH(AC)}$ to $V_{OL(AC)}$	–
Differential rising edge (^{t}RISEdiff)	–	$V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$
Differential falling edge (^{t}FALLdiff)	–	$V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$
Output slew rate rising edge	[$V_{OH(AC)}$ - $V_{OL(AC)}$]/^{t}RISE	[$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$]/^{t}RISEdiff
Output slew rate falling edge	[$V_{OH(AC)}$ - $V_{OL(AC)}$]/^{t}FALL	[$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$]/^{t}FALLdiff
Output reference load[1]	5pf to V_{SS}	
Temperature range	T_A	

Notes: 1. V_{TT} is 0.5 × V_{CCQ}.

Table 93: Output Slew Rate Matching Ratio for NV-DDR3 Without ZQ Calibration

Drive Strength	Minimum	Maximum
Output slew rate matching ratio (pull-up to pull-down)	1.0	1.4

Notes: 1. The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the falling edge is faster than the rising edge, then divide the falling slew rate by the rising slew rate.
2. The output slew rate mismatch is verified by design and characterization; it may not be subject to production testing.

Table 94: Output Slew Rate for Single-Ended NV-DDR3 (V_{CCQ} = 1.14–1.26V) With ZQ Calibration

Output Drive Strength	Min	Max	Unit
37.5 ohms	0.7	4	V/ns
50 ohms	0.6	3.5	V/ns

Table 95: Output Slew Rate for Differential NV-DDR3 (V_{CCQ}= 1.14-1.26) With ZQ Calibration

Output Drive Strength	Min	Max	Unit
37.5 ohms	1.4	8.0	V/ns
50 ohms	1.2	7.0	V/ns

Table 96: Output Slew Rate Matching Ratio for NV-DDR3 With ZQ Calibration

Drive Strength	Minimum	Maximum
Output slew rate matching ratio (pull-up to pull-down)	1.0	1.3

Notes: 1. The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the falling edge is faster than the rising edge, then divide the falling slew rate by the rising slew rate.
2. The output slew rate mismatch is verified by design and characterization; it may not be subject to production testing.

Slew rates are measured under normal SSO conditions, with half of the DQ signals per data byte driving high and half of the DQ signals per data byte driving low. The output slew rate is measured per individual DQ signal.

Power Cycle and Ramp Requirements

Upon power-down the NAND device requires a maximum voltage and minimum time that the host must hold V_{PP}, V_{CC}, and V_{CCQ} below the voltage prior to power-on. The fastest power-up and power-down ramp allowed on Micron NAND Flash is 100mV/µs.

Table 97: Power Cycle Requirements

Parameter	Value	Unit
Maximum $V_{PP}/V_{CC}/V_{CCQ}$	100	mV
Minimum time below maximum voltage	100	ns

The NAND device will successfully power-up and power-down over the range of $V_{PP}/V_{CC}/V_{CCQ}$ slew rates for the following ranges:

V_{PP} power supply voltage = 12V/95ms : 0.126mV/µs to 100mV/µs

V_{CC} power supply voltage = 2.5V/27ms : 0.094mV/µs to 100mV/µs

V_{CCQ} power supply voltage = 1.2V/20ms: 0.060mV/µs to 100mV/µs

Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to conditions above the recommended operating range or absolute maximum rating conditions for extended periods can affect reliability.

Table 98: Absolute Maximum DC Ratings by Device

Parameter	Symbol	Min[1]	Max[1]	Unit
Voltage input	V_{IN}	-0.2	1.5	V
V_{CC} supply voltage	V_{CC}	-0.6	4.6	V
V_{CCQ} supply voltage	V_{CCQ}	-0.2	1.5	V
V_{PP} supply voltage	V_{PP}	-0.6	16.0	V
V_{REFQ} supply voltage	V_{REFQ}	-0.2	1.5	V
Storage temperature	T_{STG}	-65	+150	°C

Notes: 1. Voltage on any pin relative to V_{SS}.

Table 99: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating temperature[1]	T_{OPER}	0	–	+70	°C
V_{CC} supply voltage[2]	V_{CC}	2.35	2.5	3.6	V
V_{CCQ} supply voltage (1.2V)[2]	V_{CCQ}	1.14	1.2	1.26	V
V_{PP} 12V (10.8V Min) configuration	V_{PP}	10.8	12.0	13.2	V
V_{REFQ} supply voltage	V_{REFQ}	0.49 x V_{CCQ}	0.5 x V_{CCQ}	0.51 x V_{CCQ}	V
V_{SS} ground voltage	V_{SS}	0	0	0	V

Notes: 1. Operating temperature (T_{OPER}) is the case surface temperature on the center/top of the NAND.
2. AC Noise on the supply voltages shall not exceed +/- 3% (10kHz to 800MHz). AC and DC noise together shall stay within the Min-Max range specified in this table.

Table 100: Valid Blocks per LUN

Parameter	Symbol	Min	Max	Unit	Notes
Valid block number	NVB	2104	2224	Blocks	1

Notes: 1. Invalid blocks are blocks that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid from the factory.

Package Electrical Specification and Pad Capacitance

The capacitance delta values in Input Capacitance: 132-Ball BGA Package table measure the pin-to-pin capacitance for all LUNs within a package, including across data buses if the package has the same

number of LUNs per x8 data bus (i.e. package channel). The capacitance delta values are not measured across data buses if the package has a different number of LUNs per x8 data bus.

For Package Electrical Specifications table, Z_{IO} applies to DQ[7:0], DQS_t, DQS_c, RE_t and RE_c. TdIO RE applies to RE_t and RE_c. Td_{IO} and $Td_{IO\ Mismatch}$ applies to DQ[7:0], DQS_t and DQS_c. Mismatch and Delta values are required to be met across same data bus on given package (i.e. package channel), but not required across all channels on a given package. All other pins only need meet requirements described in the Input Capacitance: 132-Ball BGA Package Table . The DQ[7:0], DQS_t, DQS_c, RE_t and RE_c pins only need to meet the requirements in the Package Electrical Specifications Table .

For each signal group defined below for Input Capacitance: 132-Ball BGA Package table, a typical capacitance value is defined and reported for each NAND Target within a package. The signal groups include all signal group pins in a single package even if the pins belong to separate I/O channels unless the package has a different number of LUNs per x8 data bus. If the package has a different number of LUNs per x8 data bus than the signal group pins are separated per each x8 data bus.

- Signal groups for Input Capacitance: 132-Ball BGA Package table:
  - Inputs1: WE#
  - Inputs2: ALE, CLE
  - Other: CE#, WP#

Table 101: Input Capacitance: 132-Ball BGA Package

Description	Symbol	Single Die/Dual Die Package			Quad Die Package			Octal Die Package			16 Die Package			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input capacitance (WE#)	C_{WE}	–	TBD	4.7	–	TBD	7.4	–	TBD	13.0	–	TBD	24.0	pF	3
Input capacitance (ALE, CLE)	C_{IN}	–	TBD	4.7	–	TBD	7.4	–	TBD	13.0	–	TBD	24.0	pF	3
Input capacitance (CE#, WP#)	C_{OTHER}	–	–	4.7	–	–	7.4	–	–	13.0	–	-	24.0	pF	
Delta input capacitance	DC_{IN}	–	–	1.4	–	–	1.7	–	–	2	–	-	4	pF	4

Notes: 1. Verified in device characterization; not 100% tested.
2. Test conditions: T_A = 25°C, f = 100 MHz, V_{IN} = 0V.
3. Values for C_{WE} and C_{IN} (TYP) are estimates.
4. For DC_{IN} the WE# pin shall be considered its own separate group, separate from ALE and CLE.

Table 102: Package Electrical Specifications

Description	Symbol	<= 400 MT/s			533 MT/s			667 MT/s			>= 800 MT/s			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input/Output Z_{PKG}	Z_{IO}	35	–	90	35	–	90	35	–	90	35	-	90	Ohms	1

Table 102: Package Electrical Specifications (Continued)

Description	Symbol	<= 400 MT/s			533 MT/s			667 MT/s			>= 800 MT/s			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Delta Z_{PKG} for DQS_t and DQS_c	$DZ_{IO\ DQS}$	–	–	10	–	–	10	–	–	10	-	-	10	Ohms	7
Input/Output Package delay	Td_{IO}	–	–	160	–	–	160	–	–	145	-	-	130	ps	1
Input/Output Package delay	$Td_{IO\ RE}$	–	–	160	–	–	160	–	–	145	-	-	130	ps	1
Input/Output Package delay mismatch	Td_{IO} Mismatch	–	–	50	–	–	40	–	–	40	-	-	40	ps	5
Delta package delay for DQS_t and DQS_c	DZd_{IO} DQS	–	–	10	–	–	10	–	–	10	-	-	10	ps	
Delta Z_{PKG} for RE_t and RE_c	$DZ_{IO\ RE}$	–	–	10	–	–	10	–	–	10	-	-	10	Ohms	
Delta package delay for RE_t and RE_c	DC_{IO}	–	–	10	–	–	10	–	–	10	-	-	10	ps	

Notes: 1. Z_{IO} and Td_{IO} apply to DQ[7:0]. DQS_t, DQS_c, RE_t and RE_c.
2. Test conditions: T_A = 25°C, f = 100 MHz, V_{IN} = 0V.
3. Verified in device characterization; not 100% tested. The package parasitic (L & C) are validated using package only samples. The capacitance is measured with V_{CC}, V_{CCQ}, V_{SS}, V_{SSQ} shorted with all other signal pins floating. The inductance is measured with V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} shorted and all other signal pins shorted at the die side (not pin).
4. Package only impedance (Z_{PKG}) is calculated based on the L_{PKG} and C_{PKG} total for a given pin where: Z_{PKG} (total per pin) = SQRT(L_{PKG}/C_{PKG}).
5. Mismatch for Td_{IO} ($Td_{IO\ Mismatch}$) is calculated based on L_{PKG} and C_{PKG} total for a given pin where: Td_{PKG}(total per pin) = SQRT(L_{PKG} * C_{PKG}).
6. Package only delay (T_{PKG}) is calculated based on L_{PKG} and C_{PKG} total for a given pin where: Td_{PKG}(total per pin) = SQRT(L_{PKG}*C_{PKG}).
7. Delta for DQS is Absolute value of Z_{IO}(DQS_t - Z_{IO}(DQS_c)) for impedance (Z) or absolute value of Td_{IO}(DQS_t) - Td_{IO}(DQS_c) for delay (Td).

8. Delta for RE is Absolute value of Z_{IO}(RE_t - Z_{IO}(RE_c)) for impedance (Z) or absolute value of Td_{IO}(RE_t) - Td_{IO}(RE_c) for delay (Td).

Table 103: LUN Pad Specifications

Description	Symbol	All timing modes			Unit	Notes
		Min	Typ	Max		
Input/Output Pad capacitance	C_Pad_{IO}	–	1.1	1.3	pF	1
ZQ Pad capacitance	C_Pad_{ZQ}	–	1.0	1.84	pF	1
Delta Input/Output Pad capacitance for DQS_t and DQS_c	$D\_C\_Pad_{IO\ DQS}$	0	–	0.2	pF	4
Delta Input/Output Pad capacitance for RE_t and RE_c	$D\_C\_Pad_{IO\ RE}$	0	–	0.2	pF	5

Notes: 1. LUN Pad capacitances apply to DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c.
2. Verified in device characterization; not 100% tested. These parameters are not subject to a production test. They are verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} applied and all other pins floating (except the pin under test). V_{CCQ} = 1.2V, VBIAS = V_{CCQ}/2 and on-die termination off.
3. These parameters apply to monolithic LUN, obtained by de-embedding the package L & C parasitics.
4. Delta for DQS is Absolute value of C_PAD_{IO}(DQS_t) - C_PAD_{IO}(DQS_c).
5. Delta for RE is Absolute value of C_PAD_{IO}(RE_t) - C_PAD_{IO}(RE_c).

Table 104: Test Conditions

Parameter	NV-DDR3 Single-ended	NV-DDR3 Differential	Notes
Rising input transition	$V_{IL(DC)}$ to $V_{IH(AC)}$	$V_{ILdiff(DC)}$ max to $V_{IHdiff(AC)}$min	1
Falling input transition	$V_{IH(DC)}$ to $V_{IL(AC)}$	$V_{IHdiff(DC)}$ max to $V_{ILdiff(AC)}$max	1
Input rise and fall slew rates	1 V/ns	2 V/ns	–
Input timing levels	V_{REFQ}	cross-point	–
Output timing levels	V_{TT}	cross-point	4
Output load: Nominal output drive strength	50Ω to V_{TT}	50Ω to V_{TT}	2, 3

Notes: 1. The receiver will effectively switch as a result of the signal crossing the AC input level; it will remain in that status as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
2. Transmission line delay is assumed to be very small.
3. This test setup applies to all package configurations.
4. V_{TT} is 0.5 x V_{CCQ}.

Electrical Specifications – DC Characteristics and Operating Conditions (NV-DDR3)

Table 105: DC Characteristics and Operating Conditions (NV-DDR3 Interface) 1.2V V_{CCQ}

Parameter	Conditions	Symbol	Single-Plane Typ[1]	Two-Plane Typ[1]	Four-Plane Typ[1]	Max Average[1]	Max Single Operation	Unit
Array read current (active)	SLC Mode IWL Read operation - without/with V_{PP}	I_{CC1_S}[2]	25/15	–	–	45/30	45/30	mA
	SLC Mode IWLx2 Read operation - without/with V_{PP}	I_{CC1_S}[2]	–	42/24	–	61/34	71/48	
	SLC Mode operation - without/with V_{PP}	I_{CC1_S}[2]	27/17	36/22	52/30	72/46	72/46	
	TLC Mode IWL Read operation - without/with V_{PP}	I_{CC1_S}[2]	22/15	–	–	38/28	38/28	
	TLC Mode IWLx2 Read operation - without/with V_{PP}	I_{CC1_S}[2]	–	36/23	–	44/29	59/33	
	TLC Mode operation - without/with V_{PP}	I_{CC1_S}[2]	27/17	34/23	48/33	58/42	72/43	
	–	I_{CCQ1_S}	1.5			5		
Array program current (active)	SLC Mode operation - without/with V_{PP}	I_{CC2_S}[3]	28/20	34/23	45/28	61/41	61/42	mA
	TLC Mode operation - without/with V_{PP}	I_{CC2_S}[3]	29/20	37/25	52/33	63/41	69/42	
	–	I_{CCQ2_S}	2			8		
Erase current (active)	without/with V_{PP}	I_{CC3_S}[4]	19/15	22/17	26/20	38/36		mA
	–	I_{CCQ3_S}	1.5			5		
Bus idle current	–	I_{CC5_S}	5			11		mA
		I_{CCQ5_S}	5			11		mA
Current during first RESET command after power-on	–	I_{CC6}	1.5			26		mA
Power-up peak current (V_{CC})	–	$I_{CC\_Peak\_Up}$ 14	–			20		mA

Table 105: DC Characteristics and Operating Conditions (NV-DDR3 Interface) 1.2V V_{CCQ} (Continued)

Parameter	Conditions	Symbol	Single-Plane Typ[1]	Two-Plane Typ[1]	Four-Plane Typ[1]	Max Average[1]	Max Single Operation	Unit
Power-down peak current (V_{CC})	–	$I_{CC\_Peak\_Down}$[14]	–			20		mA
Power-up peak current (V_{CCQ})	–	$I_{CCQ\_Peak\_Up}$[14]	–			10		mA
Power-down peak current (V_{CCQ})	–	$I_{CCQ\_Peak\_Down}$[14]	–			15		mA
V_{PP}current (active)	SLC Mode IWL Read operation with V_{PP} during I_{CC1_S}	I_{PPA1}[2]	0.9	–	–	2.8	2.8	mA
	SLC Mode IWLx2 Read operation with V_{PP} during I_{CC1_S}	I_{PPA1}[2]	–	1.7	–	2.9	2.9	mA
	SLC Mode operation with V_{PP} during I_{CC1_S}	I_{PPA1}[2]	0.9	1.4	2.4	4.4	4.4	mA
	TLC Mode IWL Read operation with V_{PP} during I_{CC1_S}	I_{PPA1}[2]	0.6	–	–	1.8	1.8	mA
	TLC Mode IWLx2 Read operation with V_{PP} during I_{CC1_S}	I_{PPA1}[2]	–	1.2	–	1.8	2.6	mA
	TLC Mode operation with V_{PP} during I_{CC1_S}	I_{PPA1}[2]	0.7	1.0	1.6	2.2	3.6	mA
	SLC Mode operation with V_{PP} during I_{CC2_S}	I_{PPA2}[3]	0.7	1.2	2.2	4.1	4.1	mA
	TLC Mode operation with V_{PP} during I_{CC2_S}	I_{PPA2}[3]	0.8	1.3	2.1	3.0	4.1	mA
	V_{PP} is supplied and enabled during I_{CC3_S}	I_{PPA3}[4]	0.4	0.5	0.7	1.2		mA
V_{PP}current (idle)	V_{PP} is not enabled	I_{PPI}	–			10		µA
Standby current - V_{CC}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SB}	10			70		µA
Standby/ current - V_{CCQ}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SBQ}	10			50		µA
Staggered power-up current	^{t}RISE = 1ms; CLINE = 0.1µF	I_{ST}	10			10		mA

Notes: 1. All values are per die (LUN) unless otherwise specified.

2. I_{CC1}/I_{PPA1} TYP is defined as the sum the current of an array read operation measured over SR[5] = 0 time multiplied by the SR[5] = 0 time for every NAND page in a NAND block divided by the total sum SR[5] = 0 time of each NAND page in a NAND block on a fully programmed block. I_{CC1}/I_{PPA1} Max average is defined as the highest I_{CC1}/I_{PPA1} TYP value. I_{CC1}/I_{PPA1} Max single operation is defined as the maximum value during any single array read operation event measured over the time SR[5] = 0, not peak current.
3. I_{CC2}/I_{PPA2} TYP is defined as the sum the current of an array program operation measured over SR[5] = 0 time multiplied by the SR[5] = 0 time for every NAND page in a NAND block divided by the total sum SR[5] = 0 time of each NAND page in a NAND block. I_{CC2}/I_{PPA2} Max average is defined as the highest I_{CC2}/I_{PPA2} TYP value. I_{CC2}/I_{PPA2} Max single operation is defined as the maximum value during any single array program operation event measured over the time SR[5] = 0, not peak current.
4. I_{CC3}/I_{PPA3} TYP is defined as the current of an array erase operation measured over SR[5] = 0 time. I_{CC3}/I_{PPA3} Max average/Max single operation is defined as the maximum value during any single array erase operation event measured over SR[5] = 0 time, not peak current..
5. These values are for one LUN per channel configurations. Configurations that have two LUNs per channel will increase by X% per interface speed. Configurations that have four LUNs per channel will increase by Y% per interface speed.
6. For speeds up to 200 MT/s.
7. For speeds greater than 200 MT/s up to 400 MT/s.
8. For speeds greater than 400 MT/s up to 667 MT/s.
9. For speeds greater than 667 MT/s up to 800 MT/s.
10. For speeds greater than 800 MT/s up to 1200 MT/s.
11. For speeds greater than 1200 MT/s up to 1600 MT/s.
12. During I_{CC} testing, On-Die Termination (ODT) is not enabled.
13. During I_{SBQ} testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.
14. For the I_{CC_Peak} and I_{CCQ_Peak} currents the entire duration of the operation should be considered when calculating the maximum average current of the worst case 1µs subset of the operation.

Table 106: DC Characteristics and Operating Conditions (NV-DDR3 Interface) 1.2V V_{CCQ} for Die (LUN) count per CE#

Parameter	Conditions	Symbol	One Die (LUN) per CE# Typ	Two Die (LUN) per CE# Typ	Four Die (LUN) per CE# Typ	Max	Unit
I/O burst read current	$^{t}RC = {}^{t}RC$ (MIN); I_{OUT}= 0mA; Per NAND DQ[7:0] channel outputting data	I_{CC4R_S}	5.4[1]			15.8[1]	mA
			9.1[2]			17.7[2]	
			14.3[3]			25.3[3]	
			16.8[4]			28.5[4]	
			23.4[5]			38.0[5]	
			30.5[6]			48.0[6]	
		I_{CCQ4R_S}	13.8[1]	14.6[1]	15.4[1]	31.0[1]	mA
			16.6[2]	18.2[2]	22.1[2]	36.1[2]	
			27.1[3]	29.1[3]	32.9[3]	58.2[3]	
			32.2[4]	35.4[4]	40.8[4]	69.6[4]	
			47.2[5]	48.8[5]	51.7[5]	81.6[5]	
			61.5[6]	64.3[6]	67.1[6]	107.5[6]	

Table 106: DC Characteristics and Operating Conditions (NV-DDR3 Interface) 1.2V V_{CCQ} for Die (LUN) count per CE#

Parameter	Conditions	Symbol	One Die (LUN) per CE# Typ	Two Die (LUN) per CE# Typ	Four Die (LUN) per CE# Typ	Max	Unit
I/O burst write current	$^{t}DSC = {}^{t}DSC$ (MIN); Per NAND DQ[7:0] channel outputting data	I_{CC4W_S}	6.5[1]			15.2[1]	mA
			8.3[2]			15.8[2]	
			11[3]			19.6[3]	
			12.3[4]			21.5[4]	
			16.0[5]			27.0[5]	
			20.7[6]			32.0[6]	
		I_{CCQ4W_S}	5.2[1]	6.3[1]	9.2[1]	19[1]	mA
			8.8[2]	11.4[2]	16.7[2]	22.8[2]	
			14.1[3]	18.3[3]	26.7[3]	36.1[3]	
			16.6[4]	21.6[4]	31.5[4]	42.4[4]	
			23.7[5]	30.9[5]	45.4[5]	60.4[5]	
			30.9[6]	40.7[6]	59.3[6]	76.1[6]	

Notes: 1. For speeds up to 200MT/s.
2. For speeds greater than 200MT/s up to 400MT/s.
3. For speeds greater than 400MT/s up to 667MT/s.
4. For speeds greater than 667MT/s up to 800MT/s.
5. For speeds greater than 800MT/s up to 1.2GT/s.
6. For speeds greater than 1.2GT/s.
7. All values are per die (LUN) unless otherwise specified.

Electrical Specifications – DC Characteristics and Operating Conditions (V_{CCQ})

Table 107: NV-DDR3 DC Characteristics and Operating Conditions for Single-Ended Signals (1.2V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	DQ[7:0], DQS, RE#	$V_{IH(AC)}$	V_{REFQ} + 0.150	–	–	V	4
AC input low voltage		$V_{IL(AC)}$	–	–	V_{REFQ} - 0.150	V	4
AC input high voltage	ALE, CLE, WE#, CE#, WP#	$V_{IH(AC)}$	0.8 × V_{CCQ}	–	V_{CCQ} + 0.3	V	4
AC input low voltage		$V_{IL(AC)}$	–0.3	–	0.2 × V_{CCQ}	V	4

Table 107: NV-DDR3 DC Characteristics and Operating Conditions for Single-Ended Signals (1.2V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
DC input high voltage	DQ[7:0], DQS, RE#	$V_{IH(DC)}$	V_{REFQ} + 0.100	–	V_{CCQ}	V	2
DC input low voltage		$V_{IL(DC)}$	V_{SSQ}	–	V_{REFQ} - 0.100	V	2
DC input high voltage	ALE, CLE, WE#, CE#, WP#	$V_{IH(DC)}$	0.7 × V_{CCQ}	–	V_{CCQ}	V	
DC input low voltage		$V_{IL(DC)}$	V_{SSQ}	–	0.3 × V_{CCQ}	V	
Input leakage current	Any input V_{IN} = 0V to V_{CCQ}	I_{LI}	–	–	±10	µA	1
Output leakage current	DQ are disabled; V_{OUT} = V_{CCQ}	I_{LO_PD}	–	TBD	TBD	µA	5
	DQ are disabled; V_{OUT} = 0V; ODT disabled	I_{LO_PU}	–	TBD	TBD	µA	5
Output low current (R/B#)	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	–	mA	3
V_{REFQ} leakage current	V_{REFQ} = V_{CCQ}/2 (all other pins not under test = 0V)	I_{VREFQ}	–	–	±5	µA	

Notes: 1. All leakage currents are per die (LUN). For example, two die (LUNs) have a maximum leakage current of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA.
2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.
3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See Configuration Operations section for additional details.
4. See AC Overshoot/Undershoot Specifications section for AC Overshoot and Undershoot requirements.
5. Absolute leakage value per I/O per NAND LUN (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

Table 108: NV-DDR3 DC Characteristics and Operating Conditions for Differential Signals (1.2V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
Differential AC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	$V_{IH\text{-}diff(AC)}$	2 x [$V_{IH(AC)}$ - V_{REF}]	–	See Note	V	2
Differential AC input low voltage		$V_{ILdiff(AC)}$	See Note	–	2 × [V_{REF} - $V_{IL(AC)}$]	V	2
Differential DC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	$V_{IH\text{-}diff(DC)}$	2 × [$V_{IH(DC)}$ - V_{REF}]	–	See Note	V	2
Differential DC input low voltage		$V_{ILdiff(DC)}$	See Note	–	2 × [V_{REF} - $V_{IL(DC)}$]	V	2
Input leakage current	Any input V_{IN} = 0V to V_{CCQ}	I_{LI}	–	–	±10	µA	1
Output leakage current	DQ are disabled; V_{OUT} = V_{CCQ}	I_{LO_PD}	–	TBD	TBD	µA	5
	DQ are disabled; V_{OUT} = 0V; ODT disabled	I_{LO_PU}	–	TBD	TBD	µA	5
Output low current (R/B#)	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	–	mA	3

Table 108: NV-DDR3 DC Characteristics and Operating Conditions for Differential Signals (1.2V V_{CCQ})

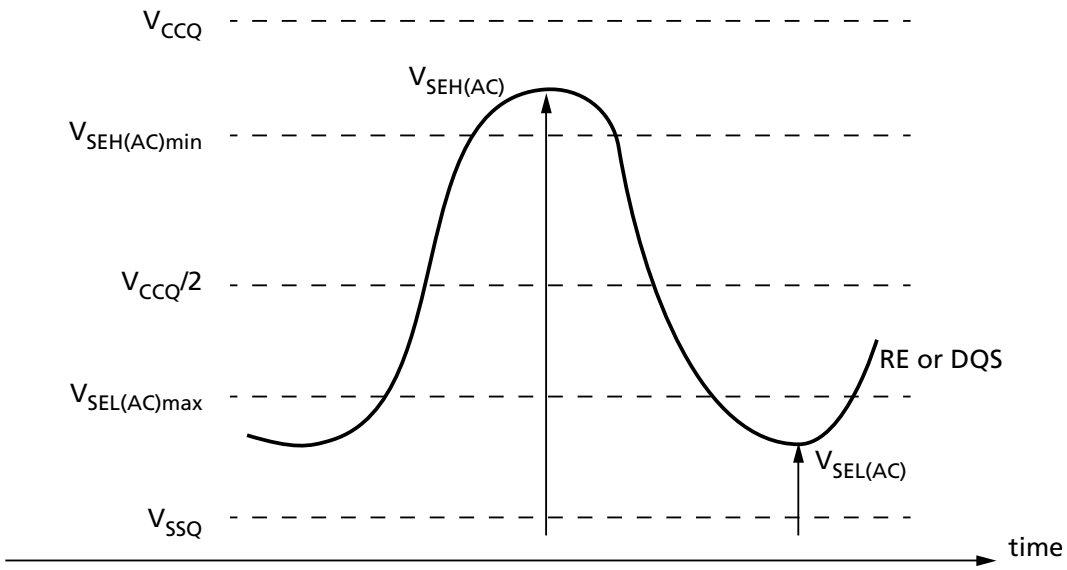
Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
V_{REFQ} leakage current	$V_{REFQ} = V_{CCQ}/2$ (all other pins not under test = 0V)	I_{VREFQ}	–	–	±5	µA	

Notes: 1. All leakage currents are per die (LUN). For example, two die (LUNs) have a maximum leakage current of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA.
2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.
3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See Configuration Operations section for additional details.
4. See AC Overshoot/Undershoot Specifications section for AC Overshoot and Undershoot requirements.
5. Absolute leakage value per I/O per NAND LUN (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (RE_t, RE_c, DQS_t, or DQS_c) shall comply with requirements for single-ended signals. RE_t and RE_c shall meet $V_{SEH(AC)}$ Min/$V_{SEL(AC)}$ Max in every half-cycle. DQS_t and DQS_c shall meet $V_{SEH(AC)}$ Min/$V_{SEL(AC)}$ Max in every half-cycle preceeding and following a valid transition.

Figure 130: Single-Ended Requirements for Differential Signals



DQ signal requirements are with respect to V_{REF}, and the single-ended components of differential signals have a requirement with respect to $V_{CCQ}/2$; This is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals, the requirement to reach $V_{SEL(AC)}$ Max, $V_{SEH(AC)}$ Min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 109: Single-Ended Levels for RE_t, RE_c, DQS_t, DQS_c for NV-DDR3 (1.2V V_{CCQ})

Parameter	Symbol	Min	Max	Unit	Notes
Single-ended high level	$V_{SEH(AC)}$	$V_{CCQ}/2$ + 0.150	See note	V	1

Table 109: Single-Ended Levels for RE_t, RE_c, DQS_t, DQS_c for NV-DDR3 (1.2V V_{CCQ})

Parameter	Symbol	Min	Max	Unit	Notes
Single-ended low level	$V_{SEL(AC)}$	See note	V_{CCQ}/2 - 0.150	V	1

Notes: 1. Values are not defined. However, single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals and for overshoot and undershoot.

Table 110: Differential AC Input/Ouput Parameters

Parameter	Symbol	Min	Max	Unit	Notes
AC differential input cross-point voltage relative to V_{CCQ}/2: NV-DDR3 interface	$V_{IX(AC)}$	0.5 x V_{CCQ} - 0.120	0.5 x V_{CCQ} + 0.120	V	1
AC differential output cross-point voltage without ZQ calibration	$V_{OX(AC)}$	0.5 x V_{CCQ} - 0.2	0.5 x V_{CCQ} + 0.2	V	2, 3, 4
AC differential output cross-point voltage with ZQ calibration	$V_{OX(AC)}$	0.5 x V_{CCQ} - 0.150	0.5 x V_{CCQ} + 0.150	V	2, 3, 4

Notes: 1. Typical value of $V_{IX(AC)}$ is expected to be 0.5 x V_{CCQ} of the transmitting device. $V_{IX(AC)}$ is expected to track variations in V_{CCQ}. $V_{IX(AC)}$ indicates the voltage at which differential input signals shall cross.
2. Typical value of $V_{OX(AC)}$ is expected to be 0.5 x V_{CCQ} of the transmitting device. $V_{OX(AC)}$ is expected to track variations in V_{CCQ}. $V_{OX(AC)}$ indicates the voltage at which differential input signals shall cross.
3. $V_{OX(AC)}$ is measured with ½ DQ signals per data byte driving logic HIGH and ½ DQ signals per data byte driving logic LOW.
4. $V_{OX(AC)}$ is verified by design and characterization; it may not be subject to production testing.

Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR3)

Table 111: AC Characteristics: NV-DDR3 Command, Address, and Data for Modes 0–4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		30		25		15		12		10		ns	
Frequency		≈33		≈40		≈66		≈83		≈100		MHz	
Command and Address													
Access window of DQ[7:0] from RE# or RE_t/RE_c	^{t}AC	3	25	3	25	3	25	3	25	3	25	ns	
ALE to data loading time	^{t}ADL	150	–	150	–	150	–	150	–	150	–	ns	13
DQ hold – command, address	^{t}CAH	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE hold	$^{t}CALH$	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	$^{t}CALS$	15	–	15	–	15	–	15	–	15	–	ns	

Table 111: AC Characteristics: NV-DDR3 Command, Address, and Data for Modes 0–4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
ALE, CLE setup with ODT enabled	^{t}CALS2	25	–	25	–	25	–	25	–	25	–	ns	
DQ setup – command, address	^{t}CAS	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	^{t}CEH	20	–	20	–	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	^{t}CEVDLY	50	–	50	–	50	–	50	–	50	–	ns	
CE# hold	^{t}CH	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	30	–	30	–	30	–	30	–	30	ns	1
CLE HIGH to output High-Z	^{t}CLHZ	–	30	–	30	–	30	–	30	–	30	ns	1
CLE to RE# LOW or RE_t/RE_c	^{t}CLR	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	^{t}CR	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c if CE# has been HIGH for >1µs	^{t}CR2	100	–	100	–	100	–	100	–	100	–	ns	
	^{t}CR2 (Read ID)	150	–	150	–	150	–	150	–	150	–	ns	14
CE# setup	^{t}CS	20	–	20	–	20	–	20	–	20	–	ns	
CE# setup for data output with ODT disabled	^{t}CS1	30	–	30	–	30	–	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	^{t}CS2	40	–	40	–	40	–	40	–	40	–	ns	17
CE# low to VOLUME SELECT (E1h)	^{t}CSVOL	100	–	100	–	100	–	100	–	100	–	ns	
CE# setup time to DQS_t low after CE# has been HIGH for >1µs	^{t}CD	100	–	100	–	100	–	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	^{t}CSD	10	–	10	–	10	–	10	–	10	–	ns	
Ready to data output	^{t}RR	20	–	20	–	20	–	20	–	20	–	ns	
WE# HIGH to R/B# LOW	^{t}WB	–	100	–	100	–	100	–	100	–	100	ns	16

Table 111: AC Characteristics: NV-DDR3 Command, Address, and Data for Modes 0–4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
WE# cycle time	^{t}WC	25	–	25	–	25	–	25	–	25	–	ns	
WE# HIGH pulse width	^{t}WH	11	–	11	–	11	–	11	–	11	–	ns	
Command cycle to data output	^{t}WHR	80	–	80	–	80	–	80	–	80	–	ns	
Address cycle to data output for training	^{t}WHRT	400	–	400	–	400	–	400	–	400	–	ns	
WE# LOW pulse width	^{t}WP	11	–	11	–	11	–	11	–	11	–	ns	
WP# transition to command cycle	^{t}WW	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	^{t}VDLY	50	–	50	–	50	–	50	–	50	–	ns	
Jitter													
The deviation of a given ^{t}DQS (abs)/^{t}DSC (abs) from a ^{t}DQS (avg)/^{t}DSC (avg)	^{t}JITper (DQS)	–2.4	2.4	–2.0	2.0	–1.2	1.2	–1.0	1.0	–0.8	0.8	ns	3, 5, 7
Deviation of a given ^{t}RC (abs)/^{t}DSC (abs) from a ^{t}RC (avg)/^{t}DSC (avg)	^{t}JITper (RE#)	–1.8	1.8	–1.5	1.5	–0.9	0.9	–0.75	0.75	–0.6	0.6	ns	3, 5, 7
Cycle to cycle jitter for DQS	^{t}JITcc (DQS)	–	4.8	–	4.0	–	2.4	–	2.0	–	1.6	ns	3, 6
Cycle to cycle jitter for RE#	^{t}JITcc (RE#)	–	3.6	–	3.0	–	1.8	–	1.5	–	1.2	ns	3, 6
Data Input													
DQS setup time for data input start	^{t}CDQSS	30	–	30	–	30	–	30	–	30	–	ns	
DQS hold time for data input burst end	^{t}CDQSH	100	–	100	–	100	–	100	–	100	–	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE, and CE# LOW during data burst	^{t}DBS	5	–	5	–	5	–	5	–	5	–	ns	

Table 111: AC Characteristics: NV-DDR3 Command, Address, and Data for Modes 0–4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Data In hold	^{t}DH	4.0	–	3.3	–	2.0	–	1.1	–	0.7	–	ns	10
Data In setup	^{t}DS	4.0	–	3.3	–	2.0	–	1.1	–	0.7	–	ns	10
DQ input pulse width	$^{t}DIPW$	0.31	–	0.31	–	0.31	–	0.31	–	0.31	–	^{t}DSC (avg)	12
DQS input high pulse width	$^{t}DQSH$	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^{t}DSC (avg)	
DQS input low pulse width	$^{t}DQSL$	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^{t}DSC (avg)	
Average DQS cycle time	^{t}DSC (avg) or ^{t}DSC	30	–	25	–	15	–	12	–	10	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	^{t}DSC (abs)	^{t}DSC (abs) MIN = ^{t}DSC (avg) + $^{t}JITper(DQS)$ MIN ^{t}DSC (abs) MAX = ^{t}DSC (avg) + $^{t}JITper(DQS)$ MAX										ns	
DQS write preamble with ODT disabled	$^{t}WPRE$	15	–	15	–	15	–	15	–	15	–	ns	
DQS write preamble with ODT enabled	$^{t}WPRE2$	25	–	25	–	25	–	25	–	25	–	ns	
DQS write postamble	$^{t}WPST$	6.5	–	6.5	–	6.5	–	6.5	–	6.5	–	ns	
DQS write postamble hold time	$^{t}WPSTH$	25	–	25	–	25	–	25	–	25	–	ns	
Data Output													
Access window of DQ[7:0] from RE# or RE_t/RE_c	^{t}AC	3	25	3	25	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE, and CE# LOW during data burst	^{t}DBS	5	–	5	–	5	–	5	–	5	–	ns	
DQS-DQ skew	$^{t}DQSQ$	–	2.5	–	2.0	–	1.4	–	1.0	–	0.8	ns	
Access window of DQS from RE# or RE_t/RE_c	$^{t}DQSRE$	3	25	3	25	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	$^{t}DQSD$	6	18	6	18	6	18	6	18	6	18	ns	

Table 111: AC Characteristics: NV-DDR3 Command, Address, and Data for Modes 0–4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS hold time after RE# LOW or RE_t/RE_c cros-spoint	^{t}DQSRH	5	–	5	–	5	–	5	–	5	–	ns	15
Data valid win-dow (device)	^{t}DVWd (device)	^{t}DVWd = ^{t}QH - ^{t}DQSQ										ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^{t}QH	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
DQS (DQS_t /DQS_c) output HIGH time	^{t}QSH	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
DQS (DQS_t /DQS_c) output LOW time	^{t}QSL	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
Average RE# cycle time	^{t}RC (avg) or ^{t}RC	30	–	25	–	15	–	12	–	10	–	ns	2
Absolute RE# cycle time	^{t}RC (abs)	^{t}RC (abs) MIN = ^{t}RC (avg) + ^{t}JITper(RE#) MIN ^{t}RC (abs) MAX = ^{t}RC (avg) + ^{t}JITper(RE#) MAX										ns	
Average RE# HIGH hold time	^{t}REH (avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Absolute RE# HIGH hold time	^{t}REH (abs)	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^{t}RC (avg)	
Data output to command, address, or data input	^{t}RHW	100	–	100	–	100	–	100	–	100	–	ns	
Average RE# pulse width	^{t}RP (avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Absolute RE# pulse width	^{t}RP (abs)	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^{t}RC (avg)	
Read preamble with ODT dis-abled	^{t}RPRE	15	–	15	–	15	–	15	–	15	–	ns	
Read preamble with ODT enabled	^{t}RPRE2	25	–	25	–	25	–	25	–	25	–	ns	
Read postamble	^{t}RPST	^{t}RPST MIN = ^{t}DQSRE + 0.5 * ^{t}RC ^{t}RPST MAX = –										ns	
Read postamble hold time	^{t}RPSTH	15	–	15	–	15	–	15	–	15	–	ns	

Notes: 1. ^{t}CHZ and ^{t}CLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.

2. The parameters ^{t}RC(avg) and ^{t}DSC(avg) are the average over any 200 consecutive periods and ^{t}RC(avg)/^{t}DSC(avg) min are the smallest rates allowed, with the exception of a deviation due to ^{t}JIT (per).
3. Input jitter is allowed provided it does not exceed values specified.
4. ^{t}REH(avg) and ^{t}RP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter ^{t}JIT (per) is the maximum deviation in the ^{t}RC or ^{t}DSC period from the average or nominal ^{t}RC or ^{t}DSC period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter ^{t}JITcc is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed ^{t}JITper. As long as the absolute minimum half period ^{t}RP(abs), ^{t}REH(abs), ^{t}DQSH or ^{t}DQSL is not less than 43 percent of the average cycle.
8. All timing parameter values assume differential signaling for RE# and DQS is used.
9. When the device is operated with input clock jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual ^{t}JITper in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
10. The ^{t}DS and ^{t}DH times listed are based on an input slew rate greater than or equal to 1 V/ns for single-ended signal, and based on an input slew rate greater than or equal to 2 V/ns for differential signal. If the input slew rate is less than 1 V/ns for single-ended signal, or less than 2 V/ns for differential signal, then the derating methodology shall be used.
11. When the device is operated with input RE (RE_t/RE_c) jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual input duty cycle jitter beyond 0.45 * ^{t}RC(avg) but not exceeding 0.43 * ^{t}RC(avg). Output deratings are relative to the device input RE pulse that generated the DQS pulse.
12. The parameter ^{t}DIPW is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
13. ^{t}ADL SPEC for SET FEATURES operations is 100ns.
14. ^{t}CR2(min) is 150ns for Read ID sequence only. For all other command sequences ^{t}CR2(min) requirement is 100ns.
15. ^{t}DQSRH is only required if Matrix ODT is enabled.
16. Any command (including read status commands) cannot be issued during ^{t}WB, even if R/B# or RDY is ready.
17. ^{t}CS2 shall be applied when the device has any type of ODT enabled including ODT only enabled for data input.

Table 112: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 5–7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock period		7.5		6		5		ns	
Frequency		≈133		≈166		≈200		MHz	
Command and Address									
Access window of DQ[7:0] from RE# or RE_t/RE_c	^{t}AC	3	25	3	25	3	25	ns	
ALE to data loading time	^{t}ADL	150	–	150	–	150	–	ns	13
DQ hold – command, address	^{t}CAH	5	–	5	–	5	–	ns	
ALE, CLE hold	^{t}CALH	5	–	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	^{t}CALS	15	–	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	^{t}CALS2	25	–	25	–	25	–	ns	

Table 112: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 5–7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQ setup – command, address	^{t}CAS	5	–	5	–	5	–	ns	
CE# HIGH hold time	^{t}CEH	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	$^{t}CEVDLY$	50	–	50	–	50	–	ns	
CE# hold	^{t}CH	5	–	5	–	5	–	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	30	–	30	–	30	ns	1
CLE HIGH to output High-Z	$^{t}CLHZ$	–	30	–	30	–	30	ns	1
CLE to RE# LOW or RE_t/RE_c	^{t}CLR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	^{t}CR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c if CE# has been HIGH for >1µs	$^{t}CR2$	100	–	100	–	100	–	ns	
	$^{t}CR2$ (Read ID)	150	–	150	–	150	–	ns	14
CE# setup	^{t}CS	20	–	20	–	20	–	ns	
CE# setup for data output with ODT disabled	$^{t}CS1$	30	–	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	$^{t}CS2$	40	–	40	–	40	–	ns	17
CE# low to VOLUME SELECT (E1h)	$^{t}CSVOL$	100	–	100	–	100	–	ns	
CE# setup time to DQS_t low after CE# has been HIGH for >1µs	^{t}CD	100	–	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	^{t}CSD	10	–	10	–	10	–	ns	
Ready to data output	^{t}RR	20	–	20	–	20	–	ns	
WE# HIGH to R/B# LOW	^{t}WB	–	100	–	100	–	100	ns	16
WE# cycle time	^{t}WC	25	–	25	–	25	–	ns	
WE# HIGH pulse width	^{t}WH	11	–	11	–	11	–	ns	
Command cycle to data output	^{t}WHR	80	–	80	–	80	–	ns	
Address cycle to data output for training	$^{t}WHRT$	400	–	400	–	400	–	ns	
WE# LOW pulse width	^{t}WP	11	–	11	–	11	–	ns	

Table 112: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 5–7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
WP# transition to command cycle	^{t}WW	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	^{t}VDLY	50	–	50	–	50	–	ns	
Jitter									
The deviation of a given ^{t}DQS (abs)/^{t}DSC (abs) from a ^{t}DQS (avg)/^{t}DSC (avg)	^{t}JITper (DQS)	–0.6	0.6	–0.48	0.48	–0.40	0.40	ns	3, 5, 7
The deviation of a given ^{t}RC (abs)/^{t}DSC (abs) from a ^{t}RC (avg)/^{t}DSC (avg)	^{t}JITper (RE#)	–0.45	0.45	–0.36	0.36	–0.30	0.30	ns	3, 5, 7
Cycle to cycle jitter for DQS	^{t}JITcc (DQS)	–	1.2	–	0.96	–	0.80	ns	3, 6
Cycle to cycle jitter for RE#	^{t}JITcc (RE#)	–	0.9	–	0.72	–	0.60	ns	3, 6
Data Input									
DQS setup time for data input start	^{t}CDQSS	30	–	30	–	30	–	ns	
DQS hold time for data input burst end	^{t}CDQSH	100	–	100	–	100	–	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE, and CE# LOW during data burst	^{t}DBS	5	–	5	–	5	–	ns	
Data In hold	^{t}DH	0.6	–	0.55	–	0.40	–	ns	10
Data In setup	^{t}DS	0.6	–	0.55	–	0.40	–	ns	10
DQ input pulse width	^{t}DIPW	0.31	–	0.31	–	0.31	–	^{t}DSC (avg)	12
DQS input high pulse width	^{t}DQSH	0.43	–	0.43	–	0.43	–	^{t}DSC (avg)	
DQS input low pulse width	^{t}DQSL	0.43	–	0.43	–	0.43	–	^{t}DSC (avg)	
Average DQS cycle time	^{t}DSC (avg) or ^{t}DSC	7.5	–	6	–	5	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	^{t}DSC (abs)	^{t}DSC (abs) MIN = ^{t}DSC (avg) + ^{t}JITper(DQS) MIN ^{t}DSC (abs) MAX = ^{t}DSC (avg) + ^{t}JITper(DQS) MAX						ns	
DQS write preamble with ODT disabled	^{t}WPRE	15	–	15	–	15	–	ns	

Table 112: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 5–7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQS write preamble with ODT enabled	^{t}WPRE2	25	–	25	–	25	–	ns	
DQS write postamble	^{t}WPST	6.5	–	6.5	–	6.5	–	ns	
DQS write postamble hold time	^{t}WPSTH	25	–	25	–	25	–	ns	
Data Output									
Access window of DQ[7:0] from RE# or RE_t/RE_c	^{t}AC	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE, and CE# LOW during data burst	^{t}DBS	5	–	5	–	5	–	ns	
DQS-DQ skew	^{t}DQSQ	–	0.6	–	0.5	–	0.4	ns	
Access window of DQS from RE# or RE_t/RE_c	^{t}DQSRE	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	^{t}DQSD	6	18	6	18	6	18	ns	
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	^{t}DQSRH	5	–	5	–	5	–	ns	15
Data valid window (device)	^{t}DVWd (device)	^{t}DVWd = ^{t}QH - ^{t}DQSQ						ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^{t}QH	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
DQS (DQS_t /DQS_c) output HIGH time	^{t}QSH	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
DQS (DQS_t /DQS_c) output LOW time	^{t}QSL	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
Average RE# cycle time	^{t}RC (avg) or ^{t}RC	7.5	–	6	–	5	–	ns	2
Absolute RE# cycle time	^{t}RC (abs)	^{t}RC (abs) MIN = ^{t}RC (avg) + ^{t}JITper(RE#) MIN ^{t}RC (abs) MAX = ^{t}RC (avg) + ^{t}JITper(RE#) MAX						ns	
Average RE# HIGH hold time	^{t}REH (avg)	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Absolute RE# HIGH hold time	^{t}REH (abs)	0.43	–	0.43	–	0.43	–	^{t}RC (avg)	
Data output to command, address, or data input	^{t}RHW	100	–	100	–	100	–	ns	
Average RE# pulse width	^{t}RP (avg)	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4

Table 112: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 5–7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Absolute RE# pulse width	^{t}RP (abs)	0.43	–	0.43	–	0.43	–	^{t}RC (avg)	
Read preamble with ODT disabled	^{t}RPRE	15	–	15	–	15	–	ns	
Read preamble with ODT enabled	^{t}RPRE2	25	–	25	–	25	–	ns	
Read postamble	^{t}RPST	^{t}RPST MIN = ^{t}DQSRE + 0.5 * ^{t}RC ^{t}RPST MAX = –						ns	
Read postamble hold time	^{t}RPSTH	15	–	15	–	15	–	ns	

Notes: 1. ^{t}CHZ and ^{t}CLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.
2. The parameters ^{t}RC(avg) and ^{t}DSC(avg) are the average over any 200 consecutive periods and ^{t}RC(avg)/^{t}DSC(avg) min are the smallest rates allowed, with the exception of a deviation due to ^{t}JIT (per).
3. Input jitter is allowed provided it does not exceed values specified.
4. ^{t}REH(avg) and ^{t}RP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter ^{t}JIT (per) is the maximum deviation in the ^{t}RC or ^{t}DSC period from the average or nominal ^{t}RC or ^{t}DSC period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter ^{t}JITcc is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed ^{t}JITper. As long as the absolute minimum half period ^{t}RP(abs), ^{t}REH(abs), ^{t}DQSH or ^{t}DQSL is not less than 43 percent of the average cycle.
8. All timing parameter values assume differential signaling for RE# and DQS is used.
9. When the device is operated with input clock jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual ^{t}JITper in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
10. The ^{t}DS and ^{t}DH times listed are based on an input slew rate greater than or equal to 1 V/ns for single-ended signal, and based on an input slew rate greater than or equal to 2 V/ns for differential signal. If the input slew rate is less than 1 V/ns for single-ended signal, or less than 2 V/ns for differential signal, then the derating methodology shall be used.
11. When the device is operated with input RE (RE_t/RE_c) jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual input duty cycle jitter beyond 0.45 * ^{t}RC(avg) but not exceeding 0.43 * ^{t}RC(avg). Output deratings are relative to the device input RE pulse that generated the DQS pulse.
12. The parameter ^{t}DIPW is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
13. ^{t}ADL SPEC for SET FEATURES operations is 100ns.
14. ^{t}CR2(min) is 150ns for Read ID sequence only. For all other command sequences ^{t}CR2(min) requirement is 100ns.
15. ^{t}DQSRH is only required if Matrix ODT is enabled.
16. Any command (including read status commands) cannot be issued during ^{t}WB, even if R/B# or RDY is ready.

17. ^{t}CS2 shall be applied when the device has any type of ODT enabled including ODT only enabled for data input.

Table 113: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 8–10

Parameter	Symbol	Mode 8		Mode 9		Mode 10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock period		3.75		3		2.5		ns	
Frequency		≈266		≈333		≈400		MHz	
Command and Address									
Access window of DQ[7:0] from RE# or RE_t/RE_c	^{t}AC	3	25	3	25	3	25	ns	
ALE to data loading time	^{t}ADL	150	–	150	–	150	–	ns	13
DQ hold – command, address	^{t}CAH	5	–	5	–	5	–	ns	
ALE, CLE hold	^{t}CALH	5	–	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	^{t}CALS	15	–	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	^{t}CALS2	25	–	25	–	25	–	ns	
DQ setup – command, address	^{t}CAS	5	–	5	–	5	–	ns	
CE# HIGH hold time	^{t}CEH	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	^{t}CEVDLY	50	–	50	–	50	–	ns	
CE# hold	^{t}CH	5	–	5	–	5	–	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	30	–	30	–	30	ns	1
CLE HIGH to output High-Z	^{t}CLHZ	–	30	–	30	–	30	ns	1
CLE to RE# LOW or RE_t/RE_c	^{t}CLR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	^{t}CR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c if CE# has been HIGH for >1µs	^{t}CR2	100	–	100	–	100	–	ns	
	^{t}CR2 (Read ID)	150	–	150	–	150	–	ns	14
CE# setup	^{t}CS	20	–	20	–	20	–	ns	
CE# setup for data output with ODT disabled	^{t}CS1	30	–	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	^{t}CS2	40	–	40	–	40	–	ns	17

Table 113: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 8–10

Parameter	Symbol	Mode 8		Mode 9		Mode 10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CE# low to VOLUME SELECT (E1h)	^{t}CSVOL	100	–	100	–	100	–	ns	
CE# setup time to DQS_t low after CE# has been HIGH for >1µs	^{t}CD	100	–	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	^{t}CSD	10	–	10	–	10	–	ns	
Ready to data output	^{t}RR	20	–	20	–	20	–	ns	
WE# HIGH to R/B# LOW	^{t}WB	–	100	–	100	–	100	ns	16
WE# cycle time	^{t}WC	25	–	25	–	25	–	ns	
WE# HIGH pulse width	^{t}WH	11	–	11	–	11	–	ns	
Command cycle to data output	^{t}WHR	80	–	80	–	80	–	ns	
Address cycle to data output for training	^{t}WHRT	400	–	400	–	400	–	ns	
WE# LOW pulse width	^{t}WP	11	–	11	–	11	–	ns	
WP# transition to command cycle	^{t}WW	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	^{t}VDLY	50	–	50	–	50	–	ns	
Jitter									
The deviation of a given ^{t}DQS (abs)/^{t}DSC (abs) from a ^{t}DQS (avg)/^{t}DSC (avg)	^{t}JITper (DQS)	–0.30	0.30	–0.24	0.24	–0.20	0.20	ns	3, 5, 7
The deviation of a given ^{t}RC (abs)/^{t}DSC (abs) from a ^{t}RC (avg)/^{t}DSC (avg)	^{t}JITper (RE#)	–0.225	0.225	–0.18	0.18	–0.15	0.15	ns	3, 5, 7
Cycle to cycle jitter for DQS	^{t}JITcc (DQS)	–	0.6	–	0.48	–	0.40	ns	3, 6
Cycle to cycle jitter for RE#	^{t}JITcc (RE#)	–	0.45	–	0.36	–	0.30	ns	3, 6
Data Input									
DQS setup time for data input start	^{t}CDQSS	30	–	30	–	30	–	ns	
DQS hold time for data input burst end	^{t}CDQSH	100	–	100	–	100	–	ns	

Table 113: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 8–10

Parameter	Symbol	Mode 8		Mode 9		Mode 10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE, and CE# LOW during data burst	^{t}DBS	5	–	5	–	5	–	ns	
Data In hold	^{t}DH	0.30	–	0.26	–	0.24	–	ns	10
Data In setup	^{t}DS	0.30	–	0.26	–	0.24	–	ns	10
DQ input pulse width	^{t}DIPW	0.31	–	0.31	–	0.31	–	^{t}DSC (avg)	12
DQS input high pulse width	^{t}DQSH	0.43	–	0.43	–	0.43	–	^{t}DSC (avg)	
DQS input low pulse width	^{t}DQSL	0.43	–	0.43	–	0.43	–	^{t}DSC (avg)	
Average DQS cycle time	^{t}DSC (avg) or ^{t}DSC	3.75	–	3	–	2.5	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	^{t}DSC (abs)	^{t}DSC (abs) MIN = ^{t}DSC (avg) + ^{t}JITper(DQS) MIN ^{t}DSC (abs) MAX = ^{t}DSC (avg) + ^{t}JITper(DQS) MAX						ns	
DQS write preamble with ODT disabled	^{t}WPRE	15	–	15	–	15	–	ns	
DQS write preamble with ODT enabled	^{t}WPRE2	25	–	25	–	25	–	ns	
DQS write postamble	^{t}WPST	6.5	–	6.5	–	6.5	–	ns	
DQS write postamble hold time	^{t}WPSTH	25	–	25	–	25	–	ns	
Data Output									
Access window of DQ[7:0] from RE# or RE_t/RE_c	^{t}AC	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE, and CE# LOW during data burst	^{t}DBS	5	–	5	–	5	–	ns	
DQS-DQ skew	^{t}DQSQ	–	0.350	–	0.30	–	0.25	ns	
Access window of DQS from RE# or RE_t/RE_c	^{t}DQSRE	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	^{t}DQSD	6	18	6	18	6	18	ns	
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	^{t}DQSRH	5	–	5	–	5	–	ns	15
Data valid window (device)	^{t}DVWd (device)	^{t}DVWd = ^{t}QH - ^{t}DQSQ						ns	

Table 113: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 8–10

Parameter	Symbol	Mode 8		Mode 9		Mode 10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^{t}QH	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
DQS (DQS_t /DQS_c) output HIGH time	^{t}QSH	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
DQS (DQS_t /DQS_c) output LOW time	^{t}QSL	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
Average RE# cycle time	^{t}RC (avg) or ^{t}RC	3.75	–	3	–	2.5	–	ns	2
Absolute RE# cycle time	^{t}RC (abs)	^{t}RC (abs) MIN = ^{t}RC (avg) + ^{t}JITper(RE#) MIN ^{t}RC (abs) MAX = ^{t}RC (avg) + ^{t}JITper(RE#) MAX						ns	
Average RE# HIGH hold time	^{t}REH (avg)	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Absolute RE# HIGH hold time	^{t}REH (abs)	0.43	–	0.43	–	0.43	–	^{t}RC (avg)	
Data output to command, address, or data input	^{t}RHW	100	–	100	–	100	–	ns	
Average RE# pulse width	^{t}RP (avg)	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Absolute RE# pulse width	^{t}RP (abs)	0.43	–	0.43	–	0.43	–	^{t}RC (avg)	
Read preamble with ODT disabled	^{t}RPRE	15	–	15	–	15	–	ns	
Read preamble with ODT enabled	^{t}RPRE2	25	–	25	–	25	–	ns	
Read postamble	^{t}RPST	^{t}RPST MIN = ^{t}DQSRE + 0.5 * ^{t}RC ^{t}RPST MAX = –						ns	
Read postamble hold time	^{t}RPSTH	15	–	15	–	15	–	ns	

Notes: 1. ^{t}CHZ and ^{t}CLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.
2. The parameters ^{t}RC(avg) and ^{t}DSC(avg) are the average over any 200 consecutive periods and ^{t}RC(avg)/^{t}DSC(avg) min are the smallest rates allowed, with the exception of a deviation due to ^{t}JIT (per).
3. Input jitter is allowed provided it does not exceed values specified.
4. ^{t}REH(avg) and ^{t}RP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter ^{t}JIT (per) is the maximum deviation in the ^{t}RC or ^{t}DSC period from the average or nominal ^{t}RC or ^{t}DSC period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter ^{t}JITcc is the amount the clock period can deviate from one cycle to the next.

7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed ^{t}JITper. As long as the absolute minimum half period ^{t}RP(abs), ^{t}REH(abs), ^{t}DQSH or ^{t}DQSL is not less than 43 percent of the average cycle.
8. All timing parameter values assume differential signaling for RE# and DQS is used.
9. When the device is operated with input clock jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual ^{t}JITper in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
10. The ^{t}DS and ^{t}DH times listed are based on an input slew rate greater than or equal to 1 V/ns for single-ended signal, and based on an input slew rate greater than or equal to 2 V/ns for differential signal. If the input slew rate is less than 1 V/ns for single-ended signal, or less than 2 V/ns for differential signal, then the derating methodology shall be used.
11. When the device is operated with input RE (RE_t/RE_c) jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual input duty cycle jitter beyond 0.45 * ^{t}RC(avg) but not exceeding 0.43 * ^{t}RC(avg). Output deratings are relative to the device input RE pulse that generated the DQS pulse.
12. The parameter ^{t}DIPW is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
13. ^{t}ADL SPEC for SET FEATURES operations is 100ns.
14. ^{t}CR2(min) is 150ns for Read ID sequence only. For all other command sequences ^{t}CR2(min) requirement is 100ns.
15. ^{t}DQSRH is only required if Matrix ODT is enabled.
16. Any command (including read status commands) cannot be issued during ^{t}WB, even if R/B# or RDY is ready.
17. ^{t}CS2 shall be applied when the device has any type of ODT enabled including ODT only enabled for data input.
18. Parameters ^{t}DQSQ and ^{t}QH are used to calculate overall ^{t}DVWd (^{t}DVWd = ^{t}QH - ^{t}DQSQ). Since data eye training to optimize strobe placement is expected at high I/O speeds (≥533 MT/s), ^{t}DQSQ and ^{t}QH may borrow time from each other without changing ^{t}DVWd. For example, if there exists X ps of margin on ^{t}DQSQ, then ^{t}QH can be provided with an additional X ps without changing the value of ^{t}DVWd. When timing margin is borrowed from ^{t}DQSQ to provide additional timing for ^{t}QH, the same amount of timing margin can be used for additional timing for ^{t}QSL or ^{t}QSH.

Table 114: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 11–15

Parameter	Symbol	Mode 11		Mode 12		Mode 13		Mode 14		Mode 15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		1.88		1.67		1.50		1.36		1.25		ns	
Frequency		≈532		≈600		≈666		≈733		≈800		MHz	
Command and Address													
Access window of DQ[7:0] from RE# or RE_t/RE_c	^{t}AC	3	25	3	25	3	25	3	25	3	25	ns	
ALE to data loading time	^{t}ADL	150	–	150	–	150	–	150	–	150	–	ns	13
DQ hold – command, address	^{t}CAH	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE hold	^{t}CALH	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	^{t}CALS	15	–	15	–	15	–	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	^{t}CALS2	25	–	25	–	25	–	25	–	25	–	ns	

Table 114: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 11–15

Parameter	Symbol	Mode 11		Mode 12		Mode 13		Mode 14		Mode 15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQ setup – command, address	^{t}CAS	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH hold time	^{t}CEH	20	–	20	–	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	$^{t}CEVDLY$	50	–	50	–	50	–	50	–	50	–	ns	
CE# hold	^{t}CH	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	30	–	30	–	30	–	30	–	30	ns	1
CLE HIGH to output High-Z	$^{t}CLHZ$	–	30	–	30	–	30	–	30	–	30	ns	1
CLE to RE# LOW or RE_t/RE_c	^{t}CLR	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	^{t}CR	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c if CE# has been HIGH for >1µs	$^{t}CR2$	100	–	100	–	100	–	100	–	100	–	ns	
	$^{t}CR2$ (Read ID)	150	–	150	–	150	–	150	–	150	–	ns	14
CE# setup	^{t}CS	20	–	20	–	20	–	20	–	20	–	ns	
CE# setup for data output with ODT disabled	$^{t}CS1$	30	–	30	–	30	–	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	$^{t}CS2$	40	–	40	–	40	–	40	–	40	–	ns	17
CE# low to VOLUME SELECT (E1h)	$^{t}CSVOL$	100	–	100	–	100	–	100	–	100	–	ns	
CE# setup time to DQS_t low after CE# has been HIGH for >1µs	^{t}CD	100	–	100	–	100	–	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	^{t}CSD	10	–	10	–	10	–	10	–	10	–	ns	
Ready to data output	^{t}RR	20	–	20	–	20	–	20	–	20	–	ns	

Table 114: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 11–15

Parameter	Symbol	Mode 11		Mode 12		Mode 13		Mode 14		Mode 15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
WE# HIGH to R/B# LOW	^{t}WB	–	100	–	100	–	100	–	100	–	100	ns	16
WE# cycle time	^{t}WC	25	–	25	–	25	–	25	–	25	–	ns	
WE# HIGH pulse width	^{t}WH	11	–	11	–	11	–	11	–	11	–	ns	
Command cycle to data output	^{t}WHR	80	–	80	–	80	–	80	–	80	–	ns	
Address cycle to data output for training	^{t}WHRT	400	–	400	–	400	–	400	–	400	–	ns	
WE# LOW pulse width	^{t}WP	11	–	11	–	11	–	11	–	11	–	ns	
WP# transition to command cycle	^{t}WW	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	^{t}VDLY	50	–	50	–	50	–	50	–	50	–	ns	
Jitter													
The deviation of a given ^{t}DQS (abs)/^{t}DSC (abs) from a ^{t}DQS (avg)/^{t}DSC (avg)	^{t}JITper (DQS)	Min = –0.094 Max = 0.094		Min = –0.083 Max = 0.083		Min = –0.078 Max = 0.078		Min = –0.075 Max = 0.075		Min = –0.070 Max = 0.070		ns	3, 5, 7
The deviation of a given ^{t}RC (abs)/^{t}DSC (abs) from a ^{t}RC (avg)/^{t}DSC (avg)	^{t}JITper (RE#)	Min = –0.094 Max = 0.094		Min = –0.083 Max = 0.083		Min = –0.078 Max = 0.078		Min = –0.075 Max = 0.075		Min = –0.070 Max = 0.070		ns	3, 5, 7
Cycle to cycle jitter for DQS	^{t}JITcc (DQS)	–	0.188	–	0.167	–	0.156	–	0.150	–	0.140	ns	3, 6
Cycle to cycle jitter for RE#	^{t}JITcc (RE#)	–	0.188	–	0.167	–	0.156	–	0.150	–	0.140	ns	3, 6
Data Input													
DQS setup time for data input start	^{t}CDQSS	30	–	30	–	30	–	30	–	30	–	ns	
DQS hold time for data input burst end	^{t}CDQSH	100	–	100	–	100	–	100	–	100	–	ns	

Table 114: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 11–15

Parameter	Symbol	Mode 11		Mode 12		Mode 13		Mode 14		Mode 15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE, and CE# LOW during data burst	^{t}DBS	5	–	5	–	5	–	5	–	5	–	ns	
Data In hold	^{t}DH (no training)	0.22	–	0.20	–	Not applicable. Per-DQ Write Training is required for data rates >1200 MT/s						ns	10
Data In setup	^{t}DS (no training)	0.22	–	0.20	–	Not applicable. Per-DQ Write Training is required for data rates >1200 MT/s						ns	10
Data In setup and hold window with per-DQ training (per-DQ Rx Mask)	^{t}DS + ^{t}DH (with training)	0.300	–	0.266	–	0.266	–	0.266	–	0.266	–	ns	21
DQ input pulse width	^{t}DIPW	0.33	–	0.33	–	0.33	–	0.33	–	0.33	–	^{t}DSC (avg)	12
Allowable skew between DQS and DQ at the ball	^{t}DQS2DQ (with training)	Min = –0.200 Max = 0.200										ns	20
Allowable skew between DQ signals at the ball	^{t}DQ2DQ (with training)	–	0.100	–	0.100	–	0.100	–	0.100	–	0.100	ns	20
DQS input high pulse width	^{t}DQSH	0.45	–	0.45	–	0.448	–	0.445	–	0.444	–	^{t}DSC (avg)	
DQS input low pulse width	^{t}DQSL	0.45	–	0.45	–	0.448	–	0.445	–	0.444	–	^{t}DSC (avg)	
Average DQS cycle time	^{t}DSC (avg) or ^{t}DSC	1.875	–	1.667	–	1.500	–	1.364	–	1.250	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	^{t}DSC (abs)	^{t}DSC (abs) MIN = ^{t}DSC (avg) + ^{t}JITper(DQS) MIN ^{t}DSC (abs) MAX = ^{t}DSC (avg) + ^{t}JITper(DQS) MAX										ns	
DQS write preamble with ODT disabled	^{t}WPRE	15	–	15	–	15	–	15	–	15	–	ns	
DQS write preamble with ODT enabled	^{t}WPRE2	25	–	25	–	25	–	25	–	25	–	ns	
DQS write postamble	^{t}WPST	6.5	–	6.5	–	6.5	–	6.5	–	6.5	–	ns	

Table 114: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 11–15

Parameter	Symbol	Mode 11		Mode 12		Mode 13		Mode 14		Mode 15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS write postamble hold time	^{t}WPSTH	25	–	25	–	25	–	25	–	25	–	ns	
Data Output													
Change in ^{t}DQSQ versus change in temperature	dQSQ/dT	–	–	–	–	–0.5	0.5	–0.5	0.5	–0.5	0.5	ps/°C	23
Change in ^{t}DQSQ versus change in V_{CCQ} voltage	dQSQ/dV	–	–	–	–	–0.35	0.35	–0.35	0.35	–0.35	0.35	ps/mV	23
Access window of DQ[7:0] from RE# or RE_t/RE_c	^{t}AC	3	25	3	25	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE, and CE# LOW during data burst	^{t}DBS	5	–	5	–	5	–	5	–	5	–	ns	
DQ-DQ skew	^{t}DQDQ	–	–	–	–	–	0.200	–	0.200	–	0.200	ns	22
DQS-DQ skew	^{t}DQSQ	–	0.188	–	0.167	Min = –0.150 Max = 0.250						ns	22
Access window of DQS from RE# or RE_t/RE_c	^{t}DQSRE	3	25	3	25	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	^{t}DQSD	6	18	6	18	6	18	6	18	6	18	ns	
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	^{t}DQSRH	5	–	5	–	5	–	5	–	5	–	ns	15
Data valid window (device)	^{t}DVWd (device)	^{t}DVWd = ^{t}QH - ^{t}DQSQ				Not applicable. DCC Training and per-DQ Read Training are required for data rates >1200 MT/s and the ^{t}DVWp spec shall be used.						ns	18
Data valid window (per pin)	^{t}DVWp (per pin)	0.535	–	0.475	–	0.428	–	0.389	–	0.356	–	ns	18
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^{t}QH	0.37	–	0.37	–	Not applicable. For data rates >1200 MT/s the ^{t}DQSQ, ^{t}DQDQ, and ^{t}DVWp specs shall be used.						^{t}RC (avg)	9, 11

Table 114: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 11–15

Parameter	Symbol	Mode 11		Mode 12		Mode 13		Mode 14		Mode 15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS (DQS_t /DQS_c) output HIGH time	^{t}QSH	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
DQS (DQS_t /DQS_c) output LOW time	^{t}QSL	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
Average RE# cycle time	^{t}RC (avg) or ^{t}RC	1.875	–	1.667	–	1.500	–	1.364	–	1.250	–	ns	2
Absolute RE# cycle time	^{t}RC (abs)	^{t}RC (abs) MIN = ^{t}RC (avg) + ^{t}JITper(RE#) MIN ^{t}RC (abs) MAX = ^{t}RC (avg) + ^{t}JITper(RE#) MAX										ns	
Average RE# HIGH hold time	^{t}REH (avg) (no training)	0.47	0.53	0.47	0.53	Not applicable. DCC Training and Per-DQ Read Training are required for data rates >1200 MT/s						^{t}RC (avg)	4
Absolute RE# HIGH hold time	^{t}REH (abs) (no training)	0.45	–	0.45	–	Not applicable. DCC Training and Per-DQ Read Training are required for data rates >1200 MT/s						^{t}RC (avg)	
Average RE# HIGH hold time	^{t}REH (avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Absolute RE# HIGH hold time	^{t}REH (abs) (with training)	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^{t}RC (avg)	
Data output to command, address, or data input	^{t}RHW	100	–	100	–	100	–	100	–	100	–	ns	
Average RE# pulse width	^{t}RP (avg) (no training)	0.47	0.53	0.47	0.53	Not applicable. DCC Training and Per-DQ Read Training are required for data rates >1200 MT/s						^{t}RC (avg)	4
Absolute RE# pulse width	^{t}RP (abs) (no training)	0.45	–	0.45	–	Not applicable. DCC Training and Per-DQ Read Training are required for data rates >1200 MT/s						^{t}RC (avg)	
Average RE# pulse width	^{t}RP (avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Absolute RE# pulse width	^{t}RP (abs) (with training)	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^{t}RC (avg)	
Read preamble with ODT disabled	^{t}RPRE	15	–	15	–	15	–	15	–	15	–	ns	
Read preamble with ODT enabled	^{t}RPRE2	25	–	25	–	25	–	25	–	25	–	ns	

Table 114: AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 11–15

Parameter	Symbol	Mode 11		Mode 12		Mode 13		Mode 14		Mode 15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read postamble	^{t}RPST	^{t}RPST MIN = ^{t}DQSRE + 0.5 × ^{t}RC ^{t}RPST MAX = –										ns	
Read postamble hold time	^{t}RPSTH	15	–	15	–	15	–	15	–	15	–	ns	

Notes:
1. ^{t}CHZ and ^{t}CLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.
2. The parameters ^{t}RC(avg) and ^{t}DSC(avg) are the average over any 200 consecutive periods and ^{t}RC(avg)/^{t}DSC(avg) min are the smallest rates allowed, with the exception of a deviation due to ^{t}JIT (per).
3. Input jitter is allowed provided it does not exceed values specified.
4. ^{t}REH(avg) and ^{t}RP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter ^{t}JIT (per) is the maximum deviation in the ^{t}RC or ^{t}DSC period from the average or nominal ^{t}RC or ^{t}DSC period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter ^{t}JITcc is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed ^{t}JITper. As long as the absolute minimum half period ^{t}RP(abs), ^{t}REH(abs), ^{t}DQSH or ^{t}DQSL is not less than 43 percent of the average cycle.
8. All timing parameter values assume differential signaling for RE# and DQS is used.
9. When the device is operated with input clock jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual ^{t}JITper in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
10. The ^{t}DS and ^{t}DH times listed are based on an input slew rate greater than or equal to 1 V/ns for single-ended signal, and based on an input slew rate greater than or equal to 2 V/ns for differential signal. If the input slew rate is less than 1 V/ns for single-ended signal, or less than 2 V/ns for differential signal, then the derating methodology shall be used.
11. When the device is operated with input RE (RE_t/RE_c) jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual input duty cycle jitter beyond 0.45 * ^{t}RC(avg) but not exceeding 0.43 * ^{t}RC(avg). Output deratings are relative to the device input RE pulse that generated the DQS pulse.
12. The parameter ^{t}DIPW is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
13. ^{t}ADL SPEC for SET FEATURES operations is 100ns.
14. ^{t}CR2(min) is 150ns for Read ID sequence only. For all other command sequences ^{t}CR2(min) requirement is 100ns.
15. ^{t}DQSRH is only required if Matrix ODT is enabled.
16. Any command (including read status commands) cannot be issued during ^{t}WB, even if R/B# or RDY is ready.
17. ^{t}CS2 shall be applied when the device has any type of ODT enabled including ODT only enabled for data input.
18. Parameters ^{t}DQSQ and ^{t}QH are used to calculate overall ^{t}DVWd (^{t}DVWd = ^{t}QH - ^{t}DQSQ). ^{t}DVWd is the data valid window per device per UI and is derived from [^{t}QH - ^{t}DQSQ] of each UI on a pin per device. Since data eye training to optimize strobe placement is expected at high I/O speeds (≥533 MT/s), ^{t}DQSQ and ^{t}QH may borrow time from each other without changing ^{t}DVWd. For example, if there exists X ps of margin on ^{t}DQSQ, then ^{t}QH can be provided with an additional X ps without changing the value of ^{t}DVWd. When timing margin is borrowed from ^{t}DQSQ to provide additional timing for ^{t}QH, the same amount of timing margin can be used for additional timing for ^{t}QSL or ^{t}QSH. For >800MT/s data rates, use of the ^{t}DVWp (per pin valid window) spec requires that the system performs DCC training and per-DQ Read Training for each LUN.
19. For greater than 800MT/s, warmup cycle(s) are required for both data input and output.

20. Both ^{t}DQS2DQ and ^{t}DQ2DQ are parameters used only when Write DQ training is supported. ^{t}DQS2DQ is the maximum allowable skew between DQS and DQ at the ball, while ^{t}DQ2DQ is the maximum allowable skew between DQ signals at the ball.The controller should be capable of compensating for the maximum amount of ^{t}DQS2DQ and ^{t}DQ2DQ skew during write training. Even with ^{t}DQS2DQ and ^{t}DQ2DQ, ^{t}DIPW still needs to be met.
21. The ^{t}DS + ^{t}DH (with training) spec is the Rx Mask for each DQ pin. This spec can only be used on a system with a controller with per-DQ Write Training capability. A controller with per-DQ Write Training capability is expected to adjust each DQ signal against DQS_t/DQS_c to obtain the optimum passing operating point for each DQ.
22. The ^{t}DQSQ is the worst case data output skew between DQS and DQ pins on a LUN while ^{t}DQDQ is the worst case data output skew between DQ pins on a LUN. The ^{t}DQDQ of a LUN however shall not cause ^{t}DQSQ to extend beyond the minimum and maximum ^{t}DQSQ specifications.
23. These specifications are not tested in production but guaranteed by design and characterization.

Electrical Specifications – Array Characteristics

Table 115: TLC Array Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	1	Cycles	1
ERASE BLOCK operation time	^{t}BERS	5	18	ms	7
Cache program operation time	^{t}CBSY	950	2200	µs	5
Change column setup time to data in/out or next command for both single LUN and multi LUN operation	^{t}CCS	–	–	ns	10
Dummy busy time	^{t}DBSY	–	0.5	µs	
ERASE SUSPEND operation time	^{t}ESPD	–	150	µs	
Busy time when ERASE RESUME is issued when no erase is suspended or ongoing	^{t}ESPDN	–	18	µs	
Busy time for SET FEATURES and GET FEATURES operations Feature Address < 80h	^{t}FEAT1	–	1	µs	12
Busy time for SET FEATURES and GET FEATURES operations Feature Address 80h or above	^{t}FEAT2	–	2	µs	12
CACHE LAST PAGE PROGRAM operation time	^{t}LPROG	–	–	µs	2,6
Busy time for OTP DATA PROGRAM operation if OTP is protected	^{t}OBSY	–	100	µs	
Page Buffer Transfer Busy time	^{t}PBSY	6	10	µs	
Power-on reset time	^{t}POR	1.5	4	ms	
PROGRAM PAGE operation time for Multi-Plane Program operations	^{t}PROG	–	2200	µs	5, 13
PROGRAM PAGE operation time for Single-Plane Program operations	^{t}PROG_SP	-	2820	µs	5, 13
Effective PROGRAM PAGE operation time for Multi-Plane Program operations	^{t}PROG_eff	500	–	µs	4
Effective PROGRAM PAGE operation time for Single-Plane Program operations	^{t}PROG_SP_eff	650	-	µs	4
PROGRAM SUSPEND operation time	^{t}PSPD	80	150	µs	
Busy time when PROGRAM RESUME is issued when no program is suspended or ongoing	^{t}PSPDN	–	18	µs	
READ PAGE operation time	^{t}R	52	67	µs	11
Single Bit Soft Bit Read (SBSBR) time	^{t}R_SBSBR	83	102	µs	
Auto Read Calibration time	^{t}RARC	343	430	µs	
Cache read busy time when RDY/ARDY = 1	^{t}RCBSY1	4	4.5	µs	11
Cache read busy time when RDY = 1, ARDY = 0 or 1	^{t}RCBSY2	4	67	µs	11
ERASE RESUME to ERASE SUSPEND delay	^{t}RSESPD	–	–	ms	8
PROGRAM RESUME to PROGRAM SUSPEND delay	^{t}RSPSPD	–	–	us	9

Table 115: TLC Array Characteristics (Continued)

Parameter	Symbol	Typ	Max	Unit	Notes
IWL READ operation time	^{t}RSNAP	47	59	µs	
Device reset time (Read)	^{t}RST	–	15	µs	17
Device reset time (Program)		–	30	µs	17
Device reset time (Erase)		75	150	µs	17
Reset during READ UNIQUE ID (EDh), READ OTP PAGE, and READ PARAMETER PAGE (ECh)		–	40	µs	
Reset during DQ training		–	70	µs	
Reset during Program OTP		–	150	µs	
Reset at any other time		–	5	µs	
Busy time for read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array read operation	^{t}RTABSY	9	10	µs	14
Busy time for IWL read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array IWL read operation	^{t}RTABSY_IWL	6.3	6.8	µs	15
Maximum time that the host is allowed between a ERASE SUSPEND operation and the complementary ERASE RESUME operation. Also applies during NESTED SUSPEND	^{t}SUSPEND_E	–	3.3	s	16
Maximum time that the host is allowed between a PROGRAM SUSPEND operation and the complementary PROGRAM RESUME operation	^{t}SUSPEND_P	–	100	ms	16
Full calibration time	^{t}ZQCL	–	1	µs	3
Short calibration time	^{t}ZQCS	–	0.3	µs	3

Notes:
1. The pages in the TLC Block have an NOP of 1.
2. Multi-Plane Read operation on any Shared Page Group that has a mismatched number of programmed shared pages paring across the physical planes is supported.
3. Increased time beyond TYP may result when greater than 8 LUNs share a ZQ resistor.
4. ^{t}PROG_eff excludes the time taken to enter the same data multiple-times in multi-pass programming method and is the effective time taken to program the data into the flash array.
5. In the case of a program operation that exceeds ^{t}CBSY/^{t}PROG Max, that specific NAND block may be retired by the host system.
6. ^{t}CBSY and ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).
7. In the case of an erase operation that exceeds ^{t}BERS Max, that specific NAND block may be retired by the host system.
8. ^{t}RSESPD (Min) = 2.75ms; Issuing an ERASE SUSPEND (61h) command after an ERASE RESUME (D2h) with a delay shorter than ^{t}RSESPD is not recommended but is allowed, but there may not be forward progress in the suspended erase operation. Regardless of forward progress, a single erase operation may not be suspended more than 30 times.
9. ^{t}RSPSPD (Min) = 200us; Issuing an PROGRAM SUSPEND (84h) command after an PROGRAM RESUME (13h) with a delay shorter than ^{t}RSPSPD is not recommended but is allowed, but there may not be forward progress in the suspended program operation. Regardless of forward progress, a single program operation may not be suspended more than 30 times.
10. ^{t}CCS (Min) = 400ns
11. Max spec is the worst ^{t}R time when reading a page with all shared pages programmed.

12. For Feature Address less than 80h, ^{t}FEAT time may be up to 1µs. For Feature Address 80h and above, ^{t}FEAT time may be up to 2µs.
13. When using program suspend, the observed total ^{t}PROG may exceed ^{t}PROG (Max)
14. ^{t}RTABSY applies to all array Read operations (excluding IWL). In Cache Read based operations ^{t}RTABSY still applies before the next array Cache Read operation begins.
15. ^{t}RTABSY_IWL applies to all IWL Read operations.
16. It is the host's responsibility to ensure that the time elapsed between the SUSPEND operation and the RESUME operation meets the corresponding ^{t}SUSPEND_P or ^{t}SUSPEND_E specification, or both of them in the case of Nested Suspend
17. After any array command, upon SR5/SR6 = 0, if a reset is issued, ^{t}RST will follow ^{t}RST (Program/Read/Erase). Array commands include all read operations/program operations/erase operations/copyback operations in the command set table.

Any parameters not referenced in the SLC Array Characteristics Table that would apply to SLC operations should be referenced in the TLC Array Characteristics Table .

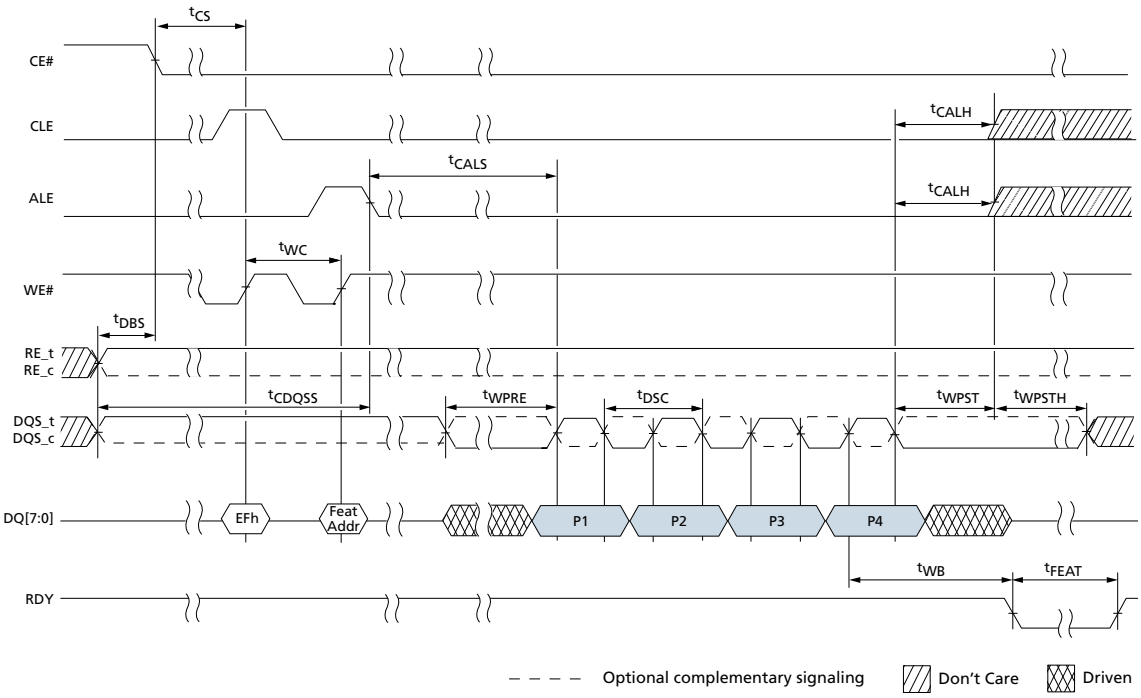
Table 116: SLC Array Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	1	Cycles	1
ERASE BLOCK operation time	^{t}BERS	6	18	ms	4
Program Cache busy	^{t}CBSY	27	700	µs	2, 3
ERASE SUSPEND operation time	^{t}ESPD	–	150	µs	
Busy time when ERASE RESUME is issued when no erase is suspended or ongoing	^{t}ESPDN	–	18	µs	
LAST PAGE PROGRAM operation time	^{t}LPROG	–	–	µs	2,3
PROGRAM PAGE operation time	^{t}PROG	120	700	µs	3 ,5, 6
PROGRAM SUSPEND operation time	^{t}PSPD	80	150	µs	3
Busy time when PROGRAM RESUME is issued when no program is suspended or ongoing	^{t}PSPDN	–	18	µs	
READ PAGE operation time	^{t}R	30	36	µs	
Cache read busy time when RDY/ARDY = 1	^{t}RCBSY1	4	4.5	µs	
Cache read busy time when RDY = 1, ARDY = 0 or 1	^{t}RCBSY2	4	36	µs	
IWL READ operation time	^{t}RSNAP	24	26	µs	
Busy time for read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array read operation	^{t}RTABSY	9	10	µs	7
Busy time for IWL read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array IWL read operation	^{t}RTABSY_IWL	6.3	6.8	µs	8
Maximum time that the host is allowed between a ERASE SUSPEND operation and the complementary ERASE RESUME operation. Also applies during NESTED SUSPEND	^{t}SUSPEND_E	–	3.3	s	9
Maximum time that the host is allowed between a PROGRAM SUSPEND operation and the complementary PROGRAM RESUME operation	^{t}SUSPEND_P	–	100	ms	9

Notes: 1. The pages in the SLC Block have an NOP of 1.
2. ^{t}CBSY and ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).
3. In the case of a program operation that exceeds ^{t}PROG/^{t}CBSY Max, that specific NAND block may be retired by the host system.
4. In the case of an erase operation that exceeds ^{t}BERS Max, that specific NAND block may be retired by the host system.
5. OTP Program operations could be up to 920us.
6. When using program suspend, the observed total ^{t}PROG may exceed ^{t}PROG (Max)
7. ^{t}RTABSY applies to all array Read operations (excluding IWL). In Cache Read based operations ^{t}RTABSY still applies before the next array Cache Read operation begins.
8. ^{t}RTABSY_IWL applies to all IWL Read operations.
9. It is the host's responsibility to ensure that the time elapsed between the SUSPEND operation and the RESUME operation meets the corresponding ^{t}SUSPEND_P or ^{t}SUSPEND_E specification, or both of them in the case of Nested Suspend

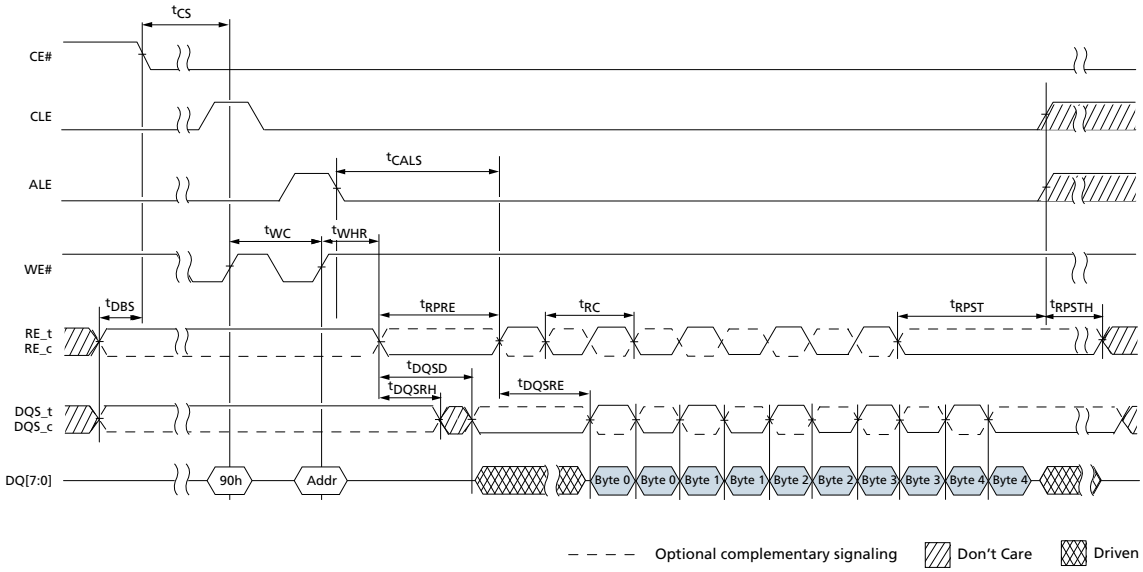
NV-DDR3 Interface Timing Diagrams

Figure 131: SET FEATURES Operation



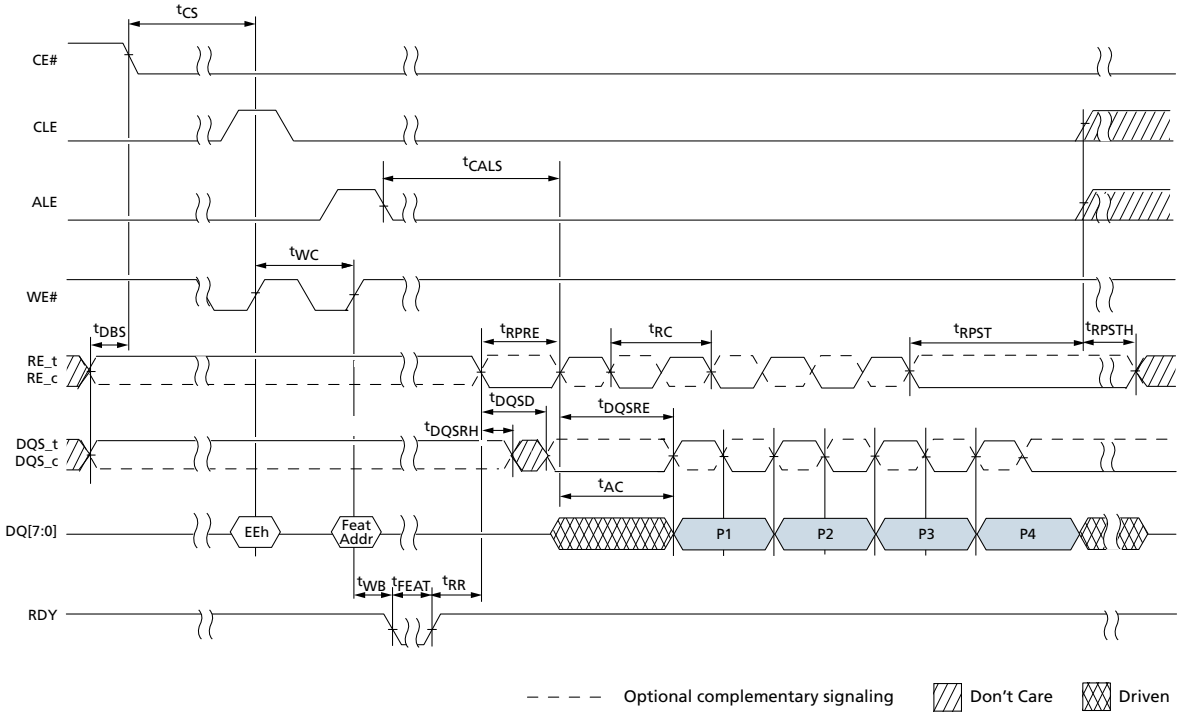
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 132: READ ID Operation



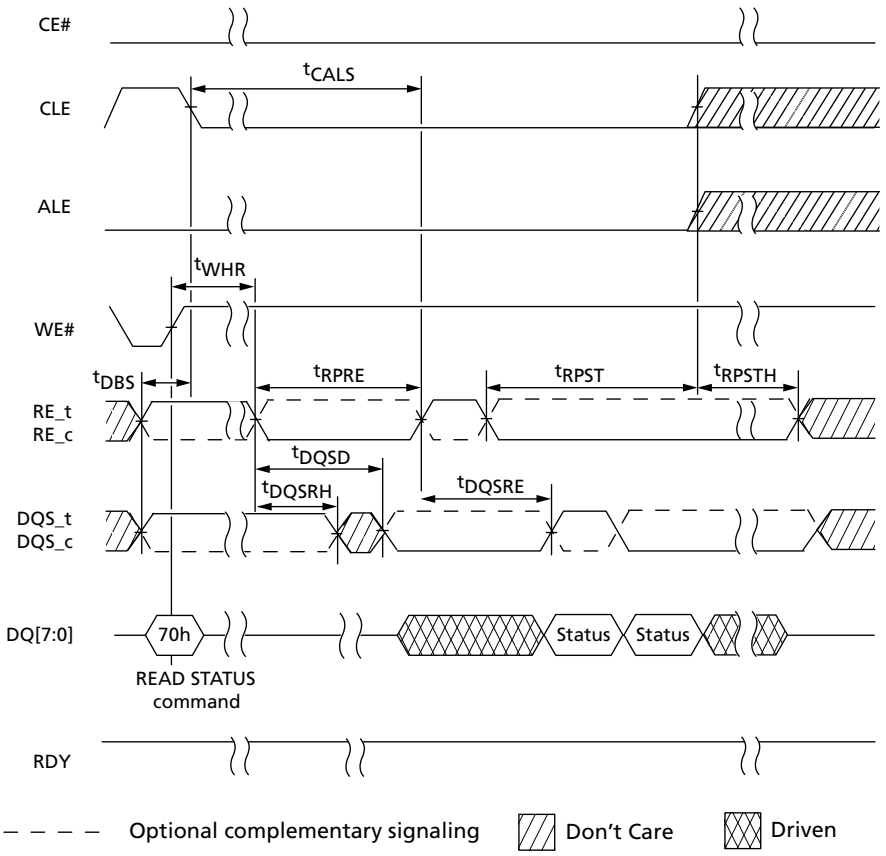
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 133: GET FEATURES Operation



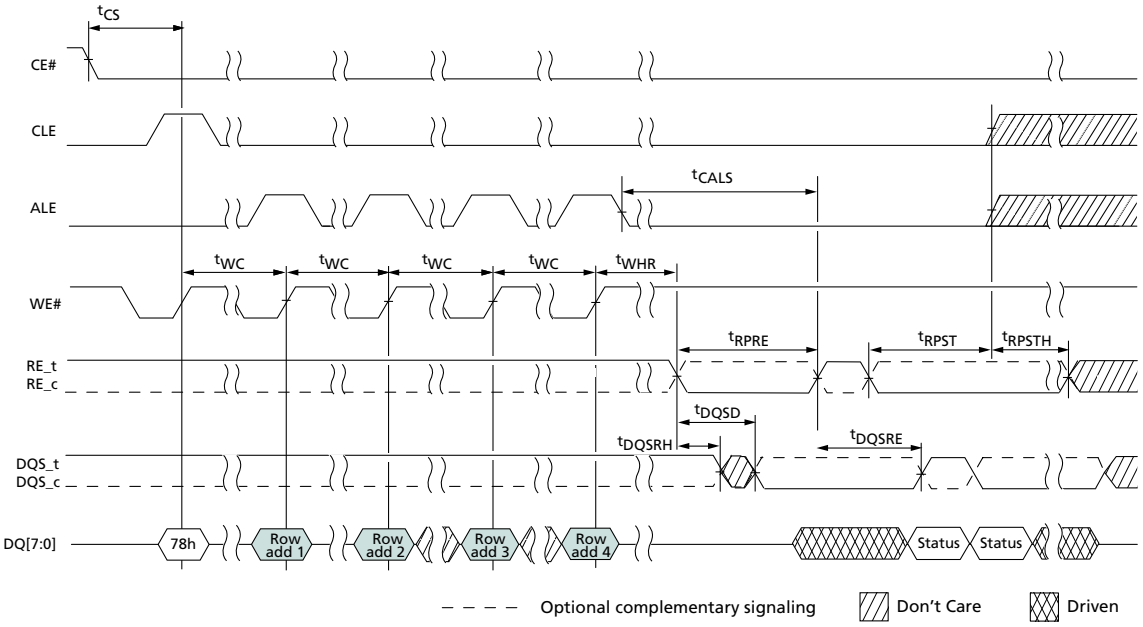
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 134: READ STATUS Cycle



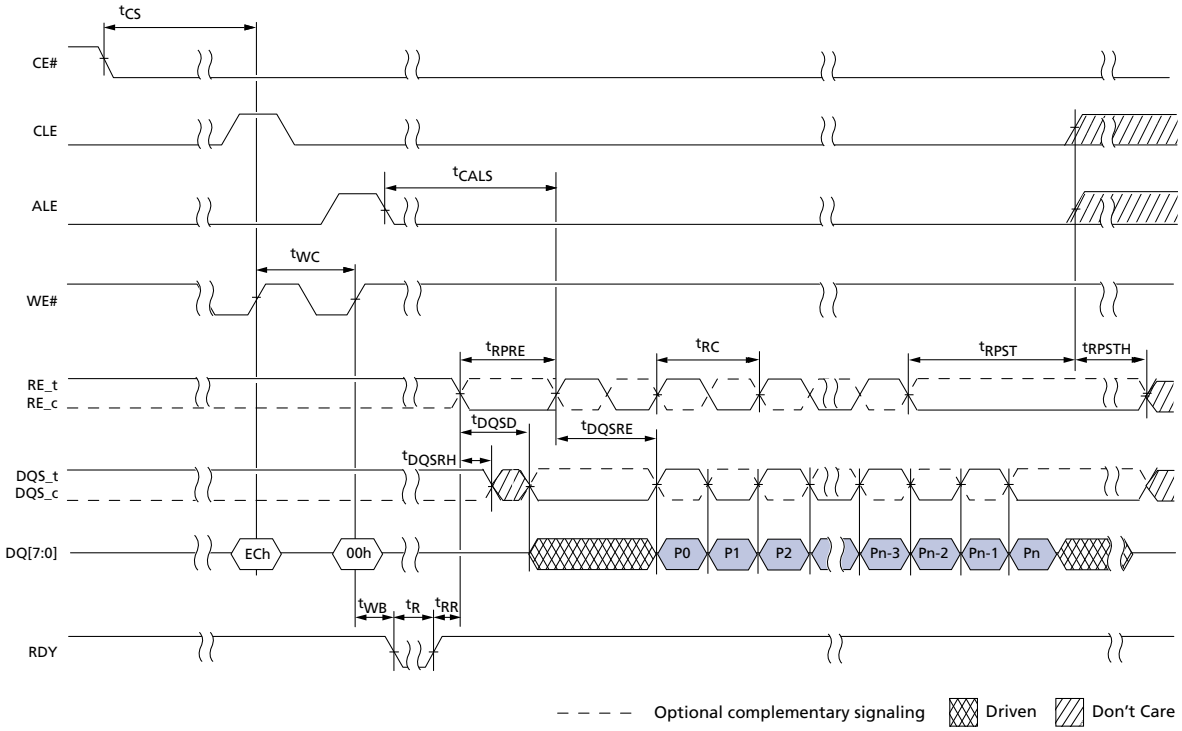
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 135: READ STATUS ENHANCED Operation



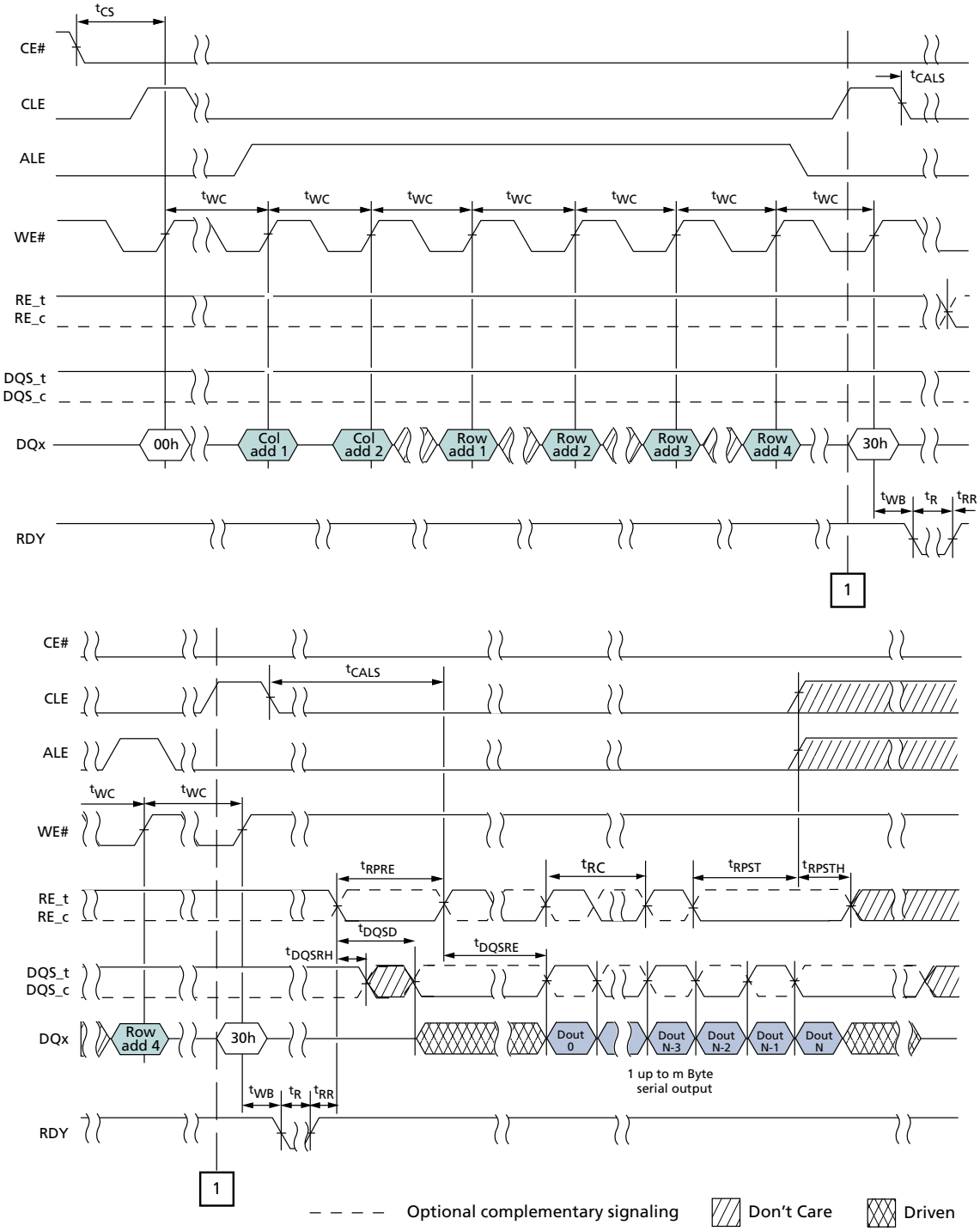
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 136: READ PARAMETER PAGE Operation



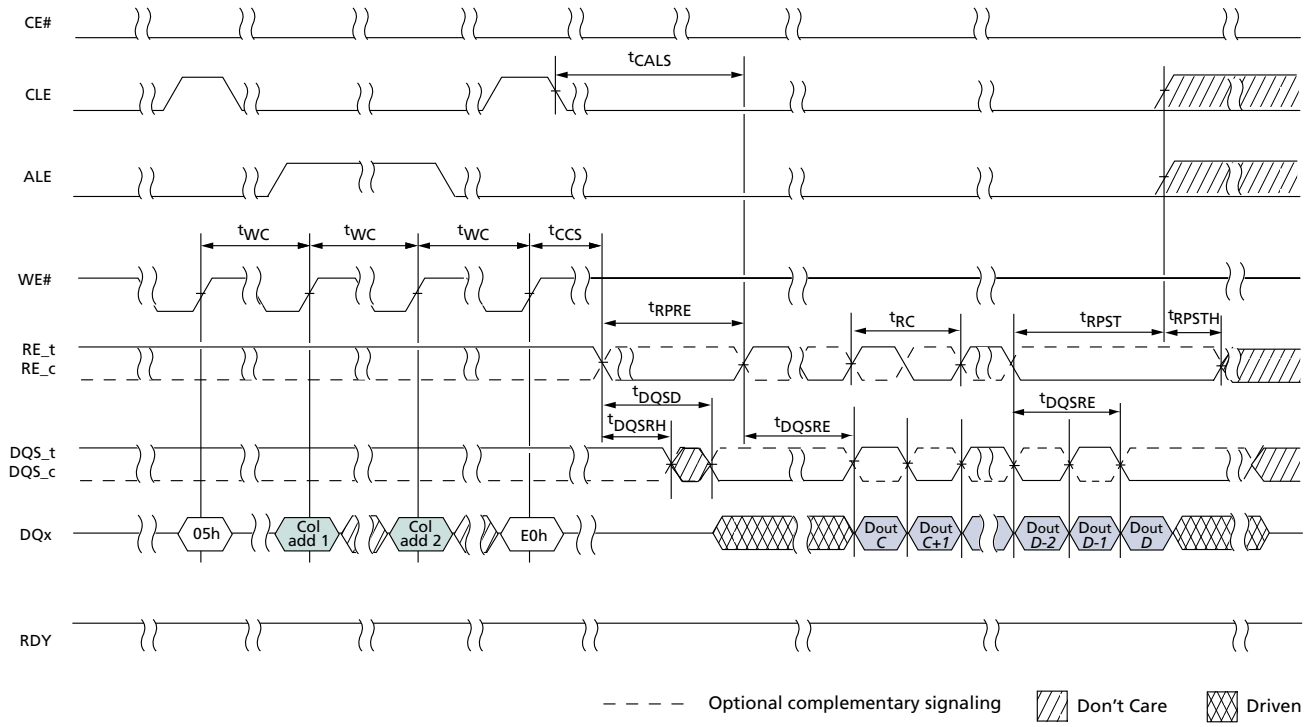
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 137: READ PAGE Operation



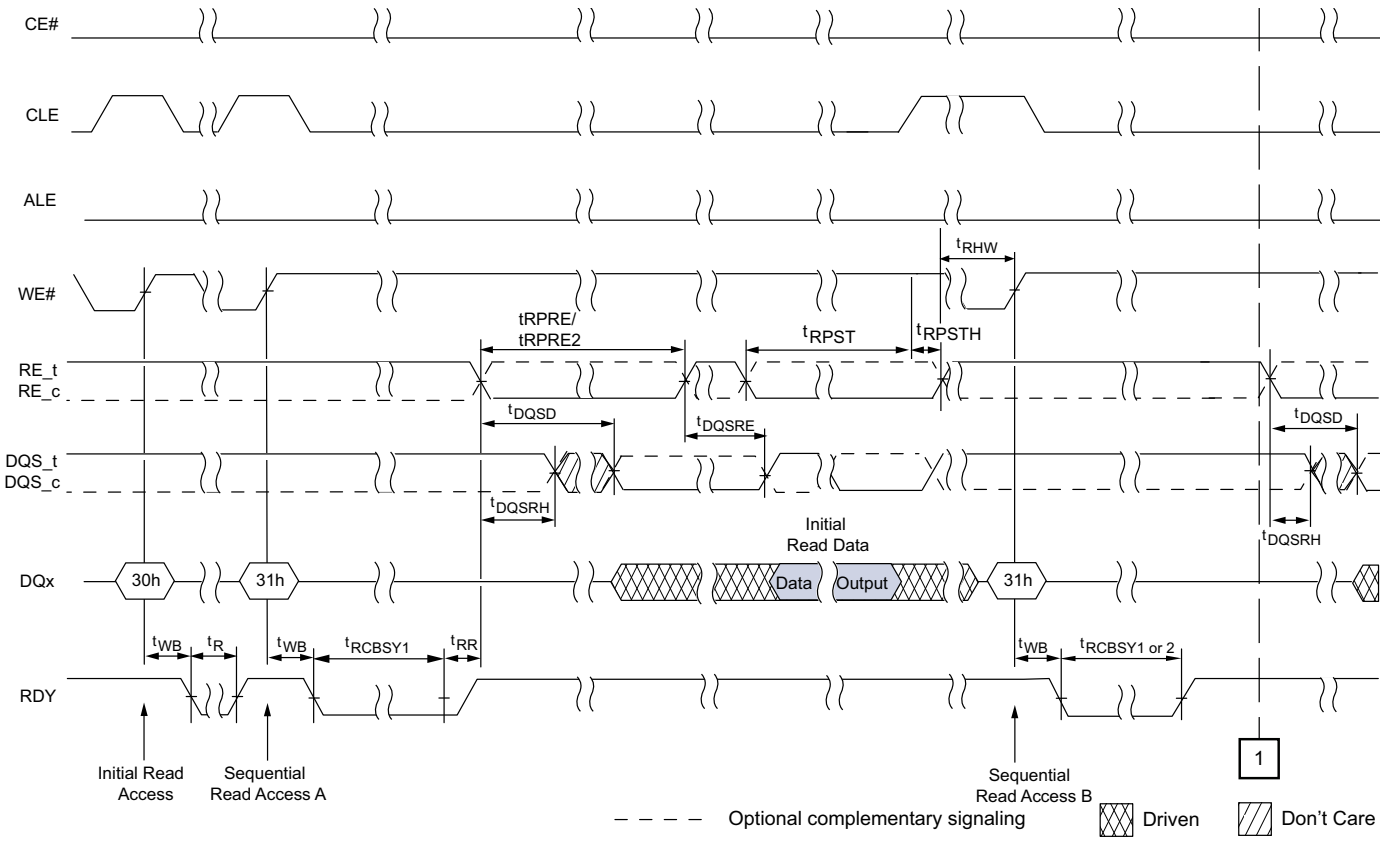
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 138: CHANGE READ COLUMN



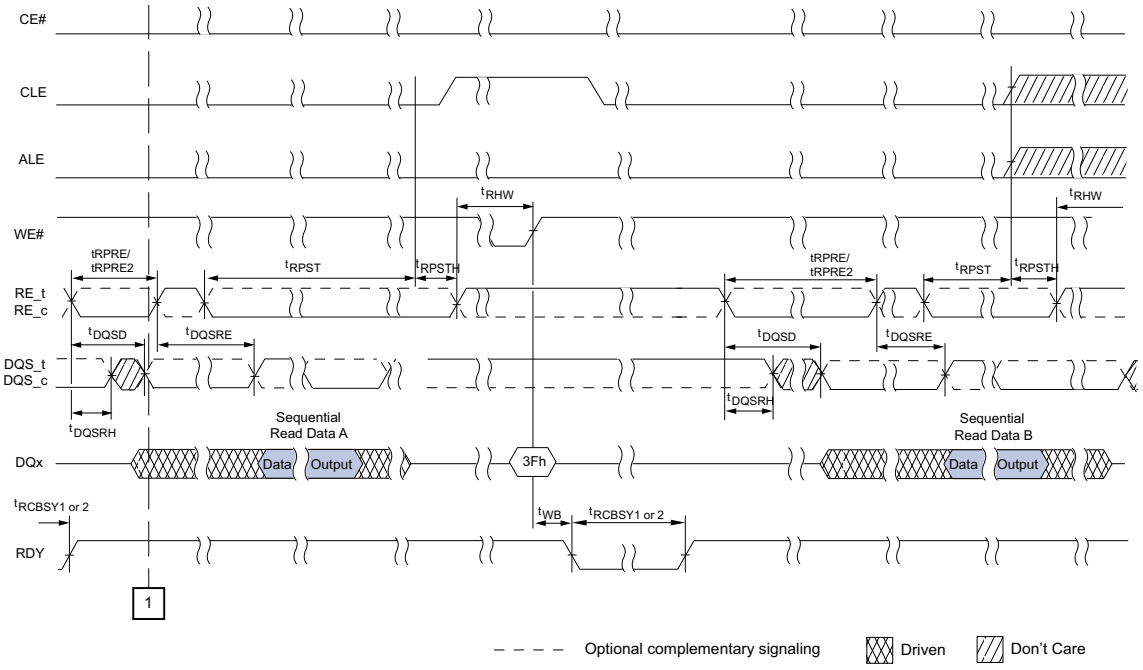
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 139: READ PAGE CACHE SEQUENTIAL (1 of 2)



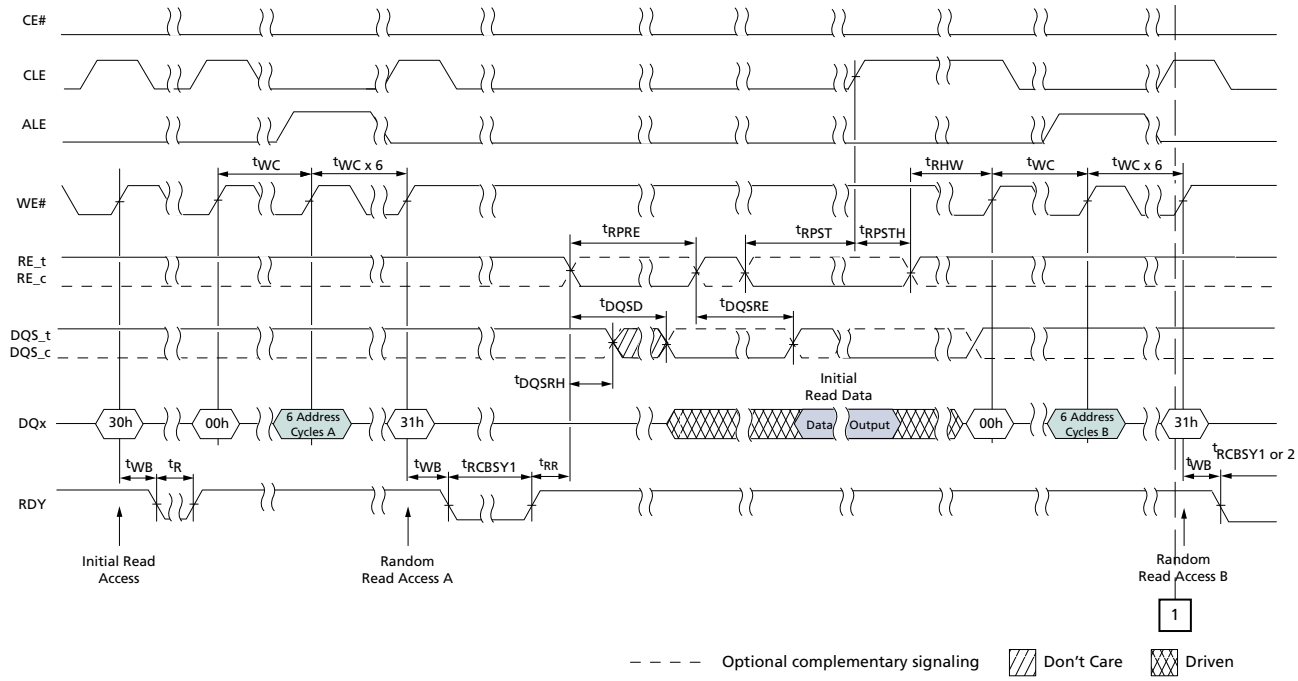
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 140: READ PAGE CACHE SEQUENTIAL (2 of 2)



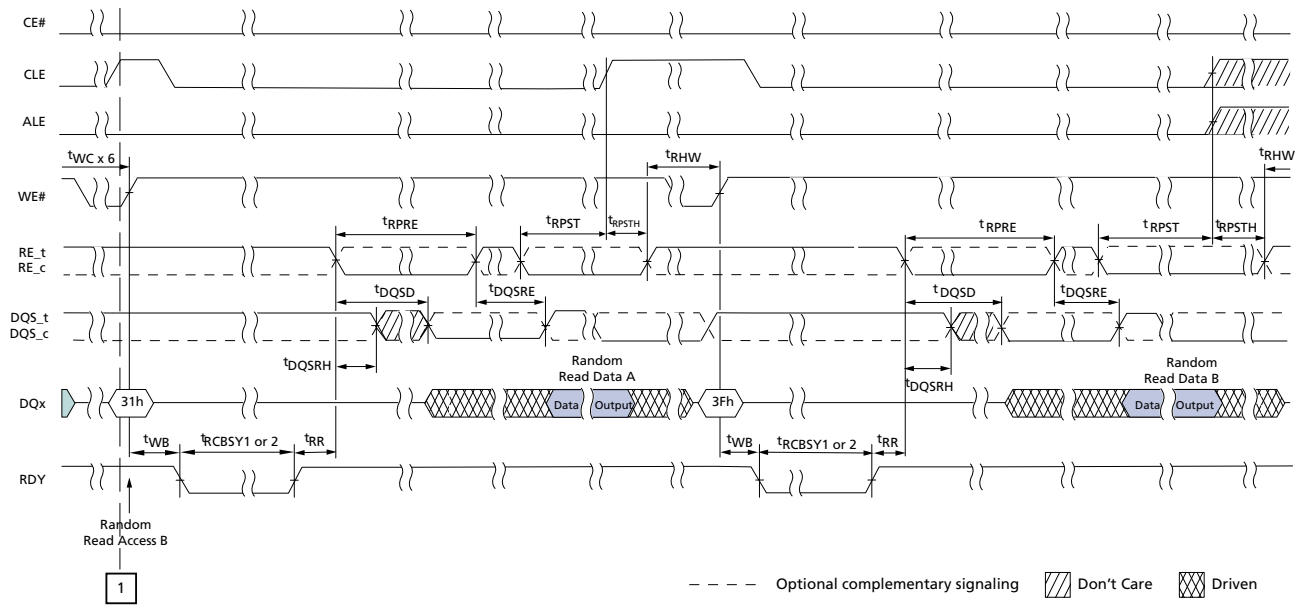
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 141: READ PAGE CACHE RANDOM (1 of 2)



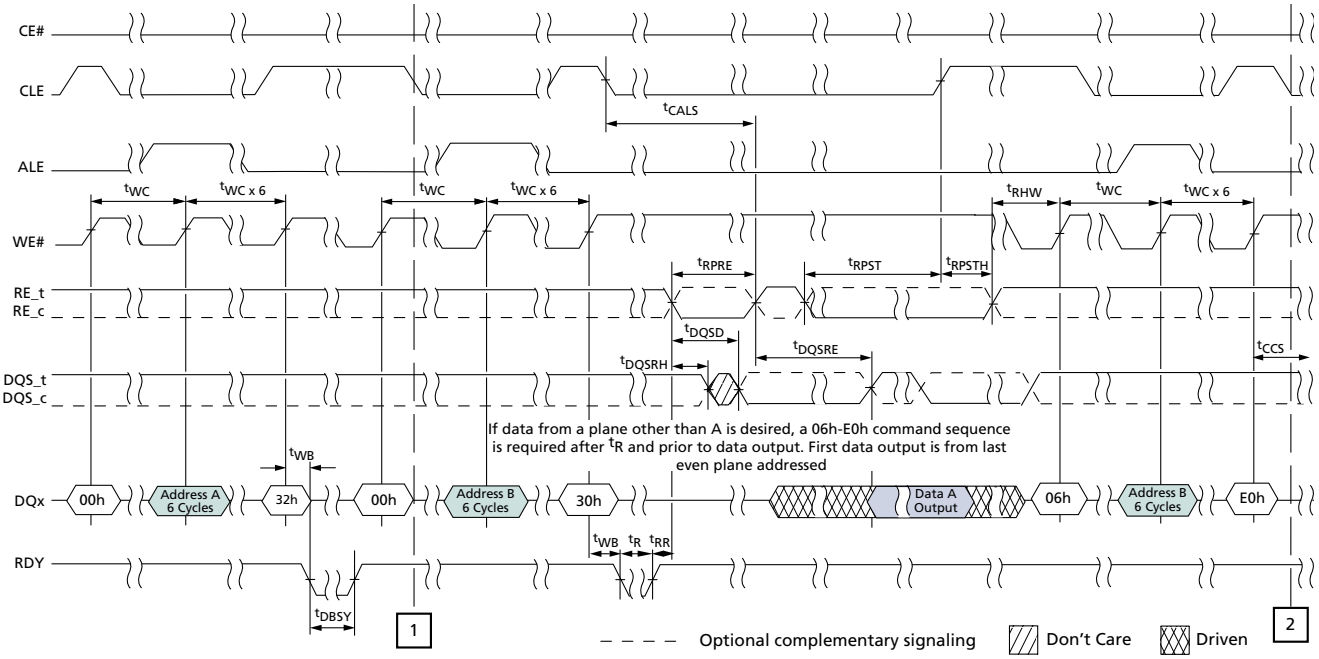
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 142: READ PAGE CACHE RANDOM (2 of 2)



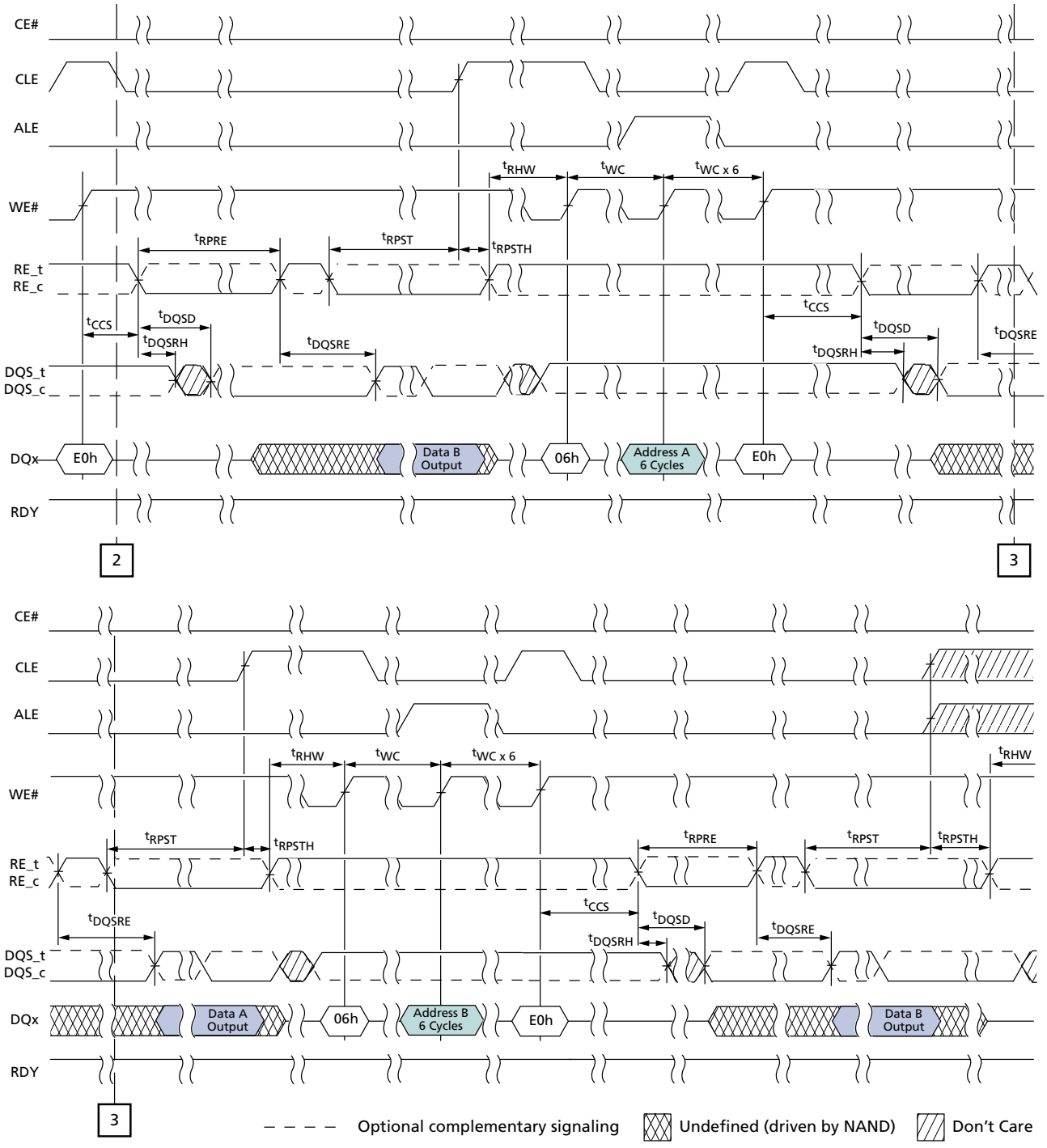
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 143: Multi-Plane Read Page (1 of 2)



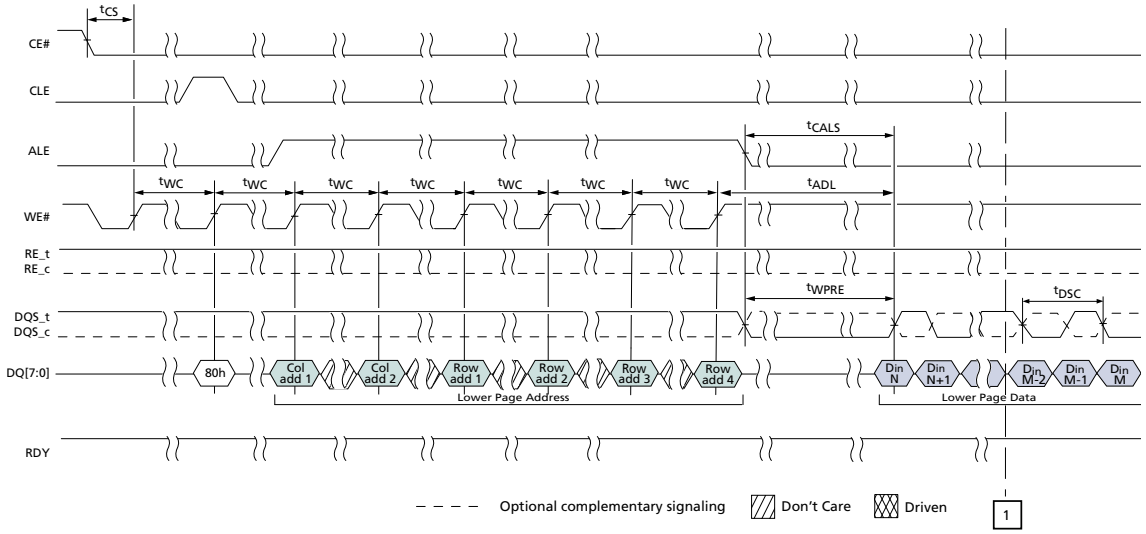
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 144: Multi-Plane Read Page (2 of 2)



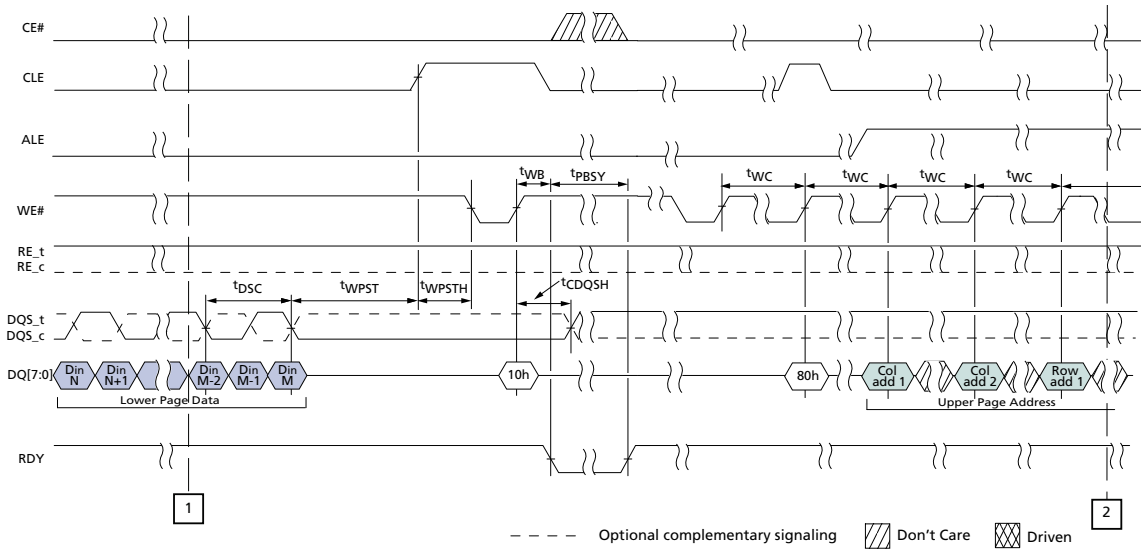
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 145: PROGRAM PAGE Operation (1 of 5)



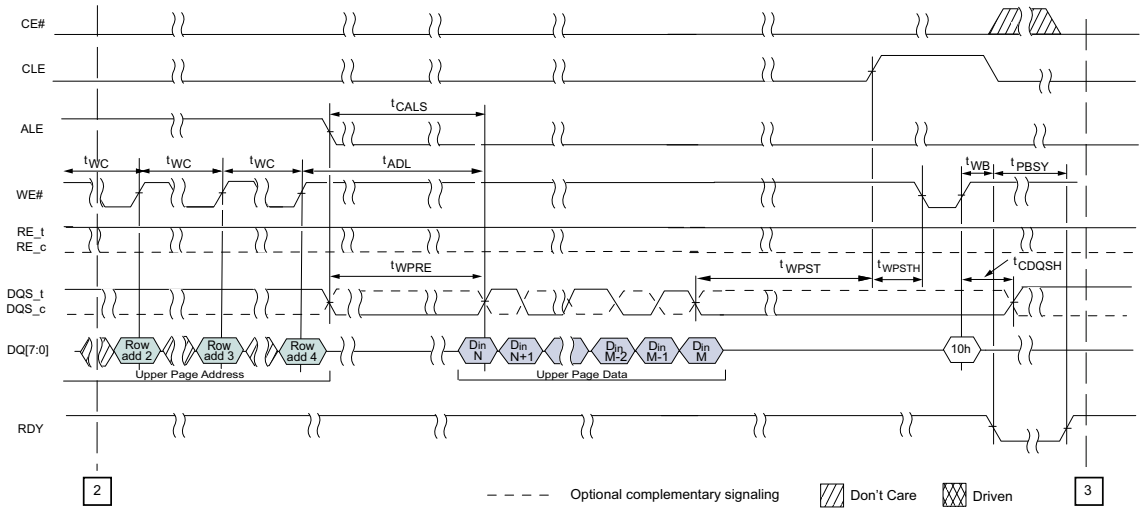
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 146: PROGRAM PAGE Operation (2 of 5)



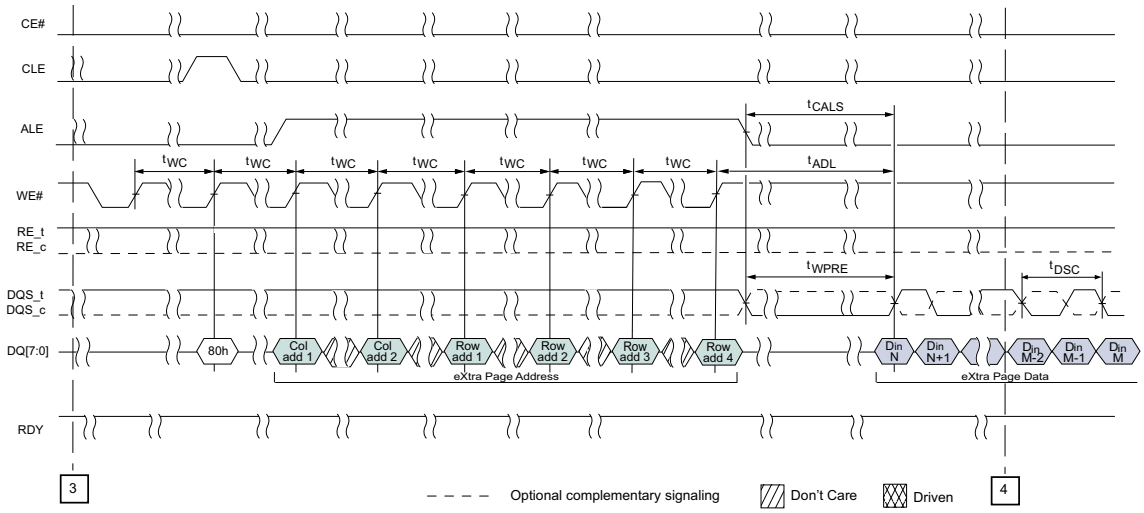
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 147: PROGRAM PAGE Operation (3 of 5)



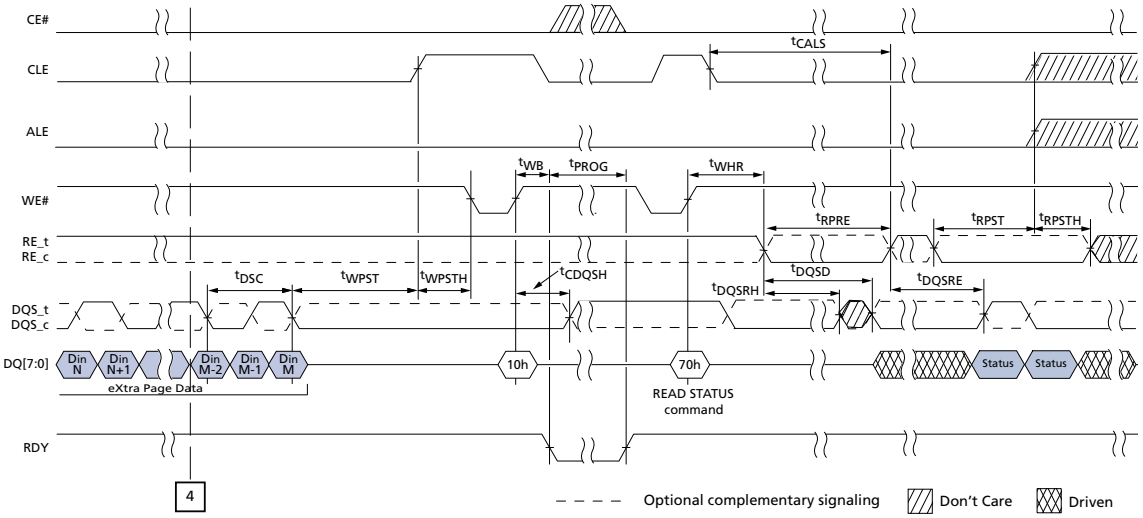
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 148: PROGRAM PAGE Operation (4 of 5)



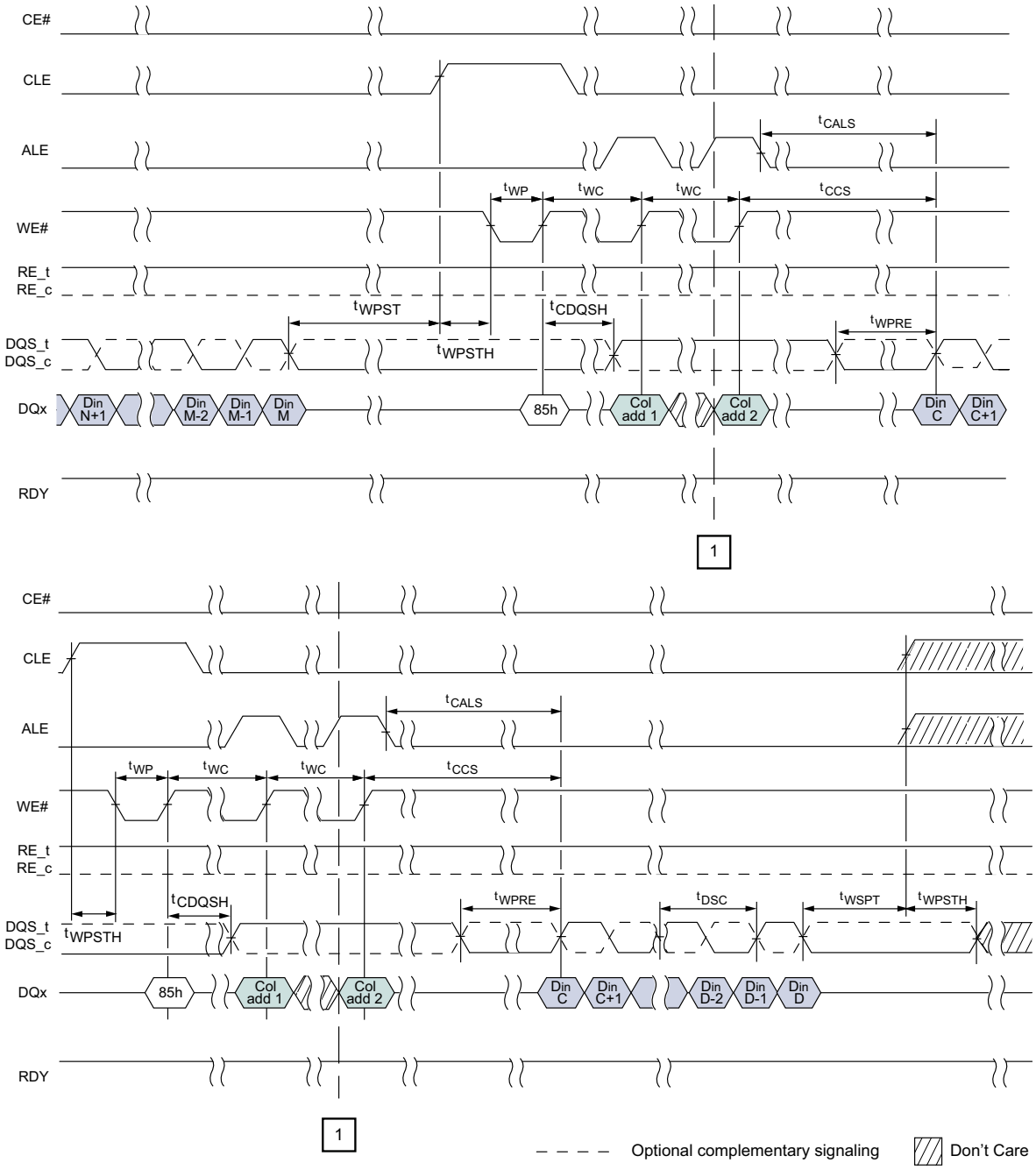
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 149: PROGRAM PAGE Operation (5 of 5)



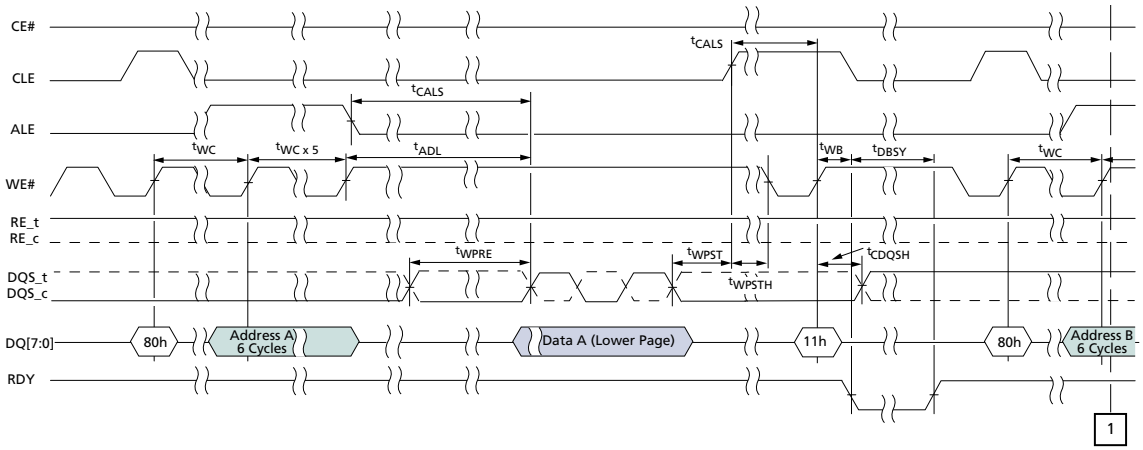
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 150: CHANGE WRITE COLUMN



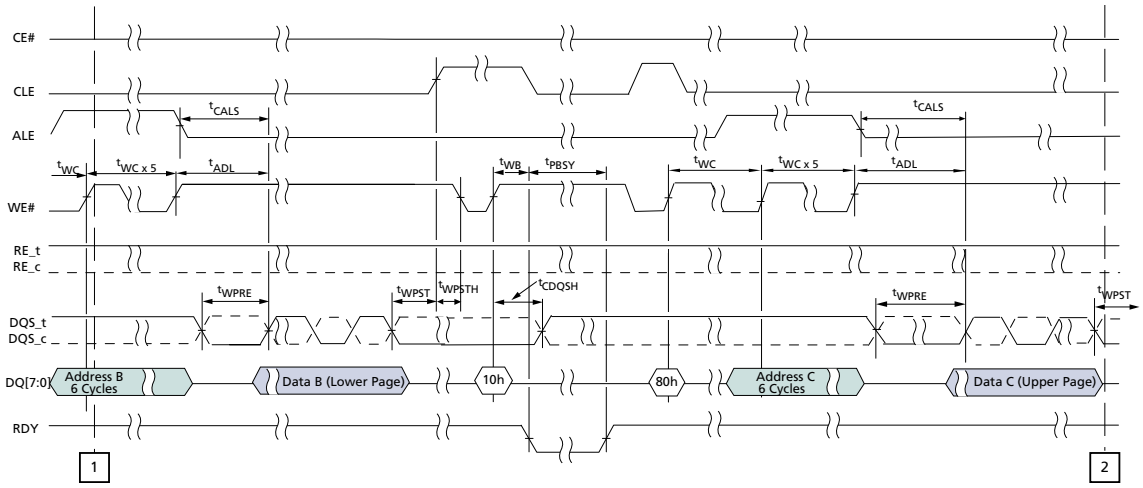
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 151: Multi-Plane Program Page (1 of 5)



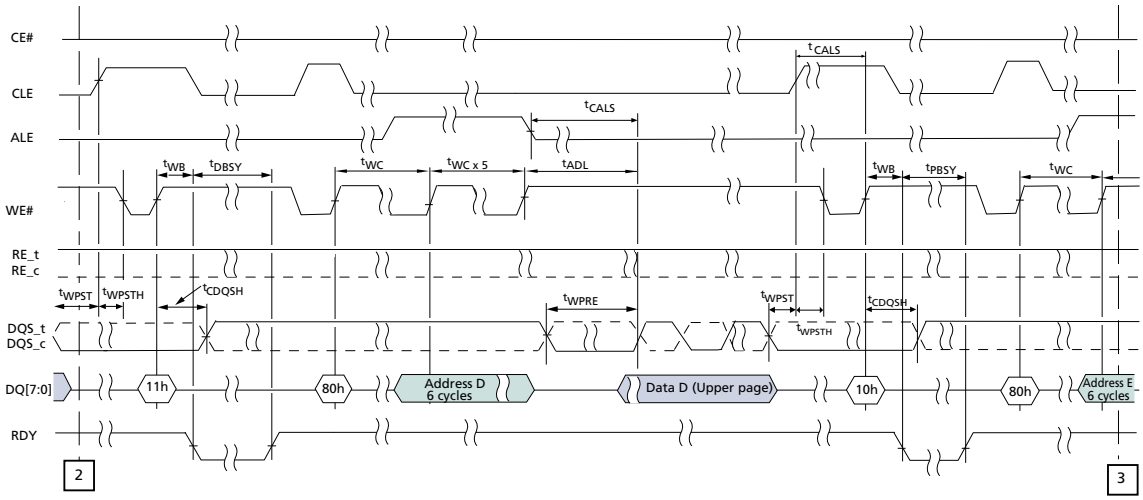
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 152: Multi-Plane Program Page (2 of 5)



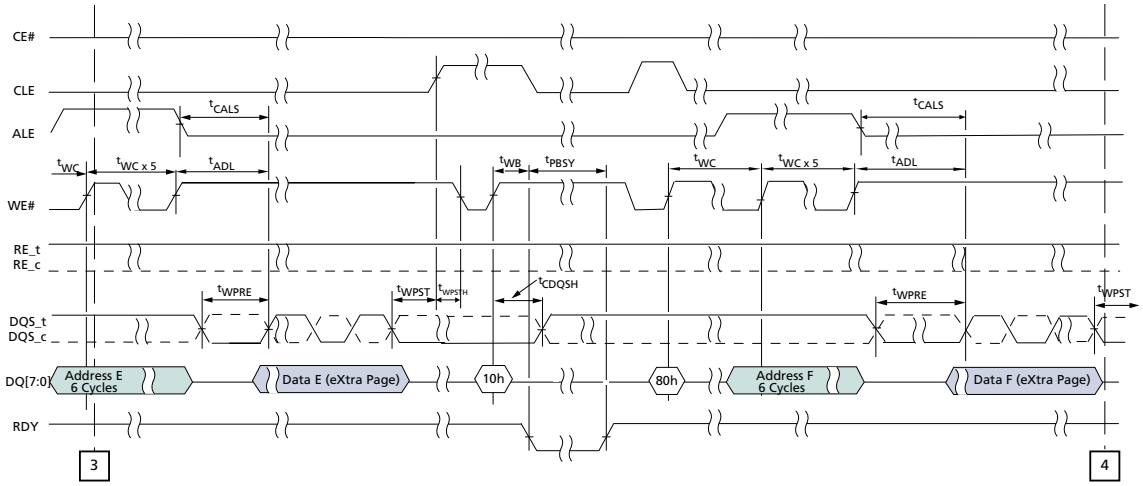
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 153: Multi-Plane Program Page (3 of 5)



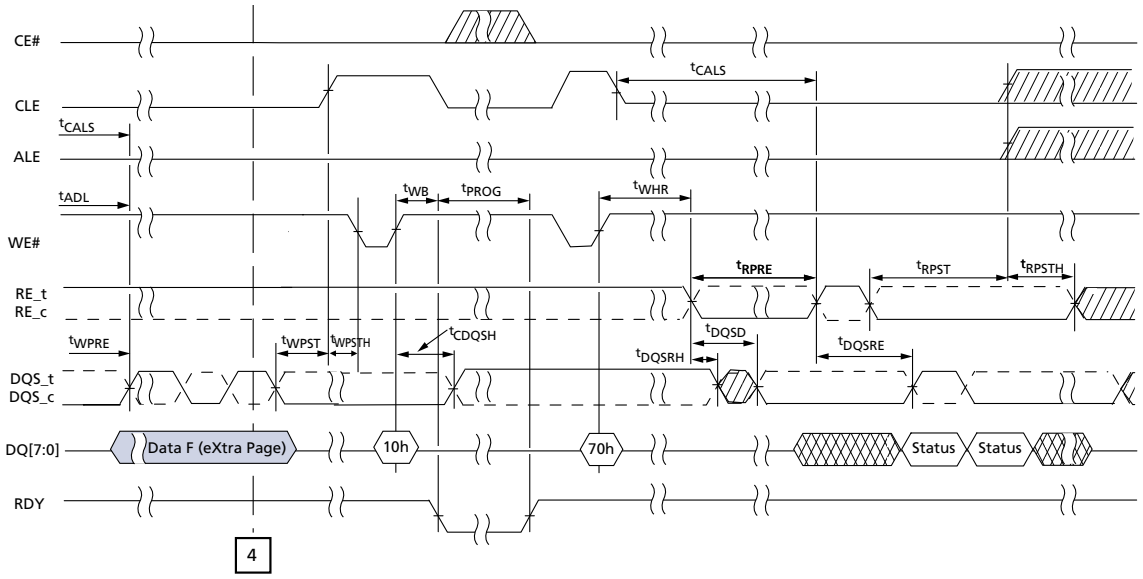
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 154: Multi-Plane Program Page (4 of 5)



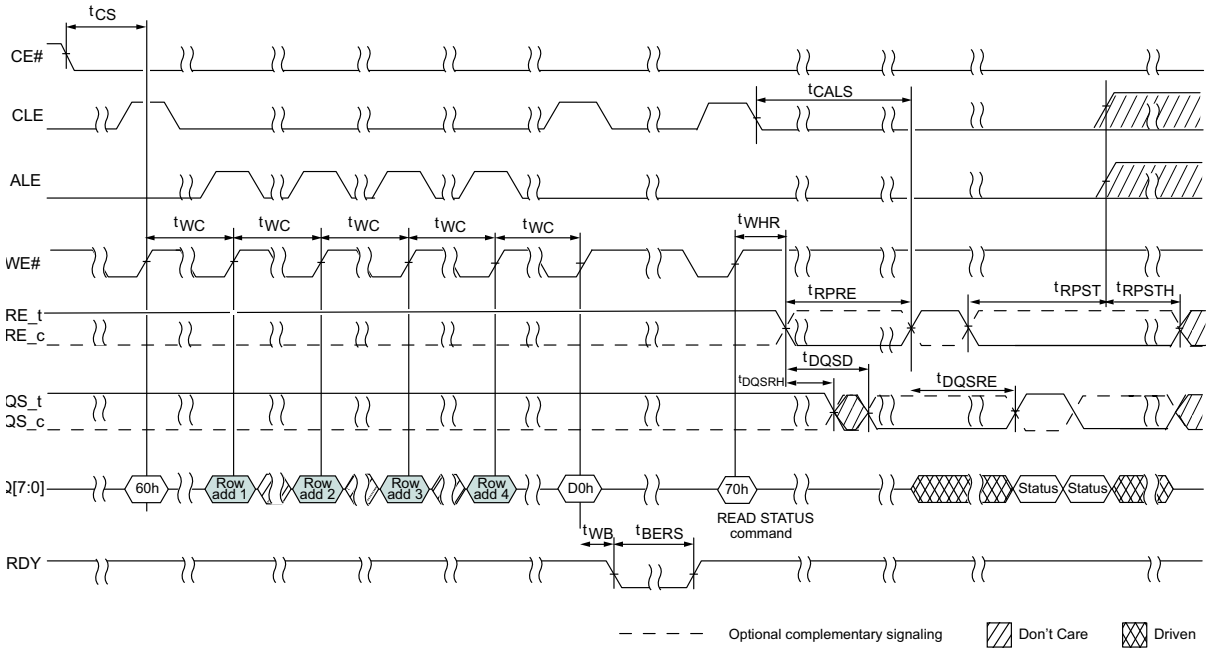
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 155: Multi-Plane Program Page (5 of 5)



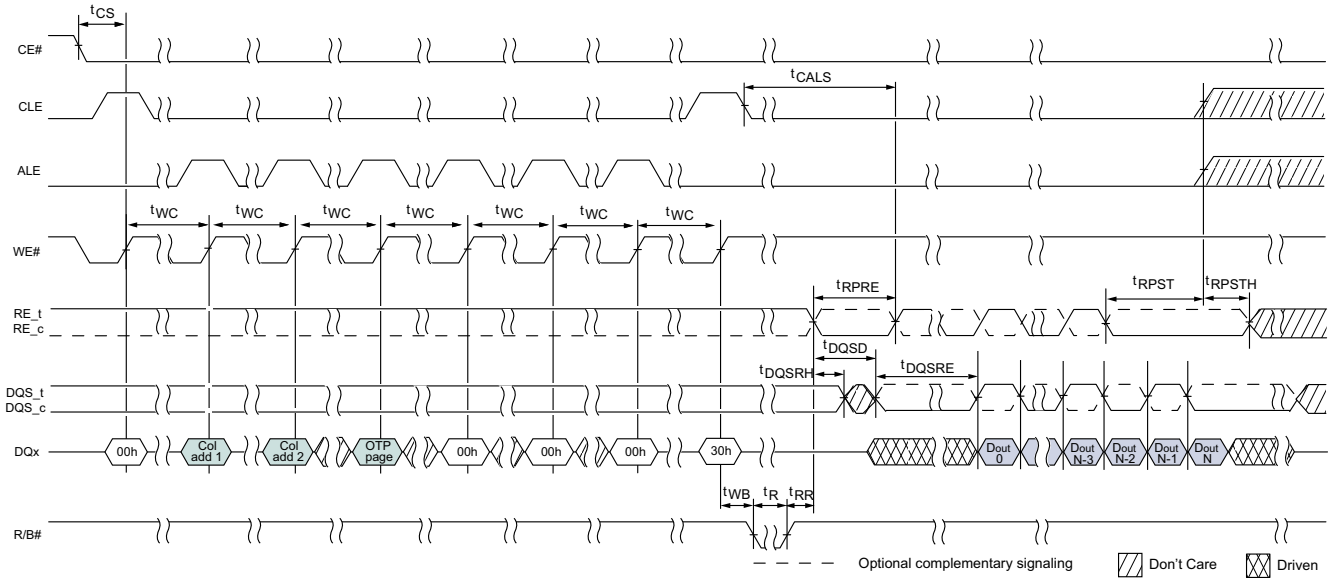
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 156: ERASE BLOCK



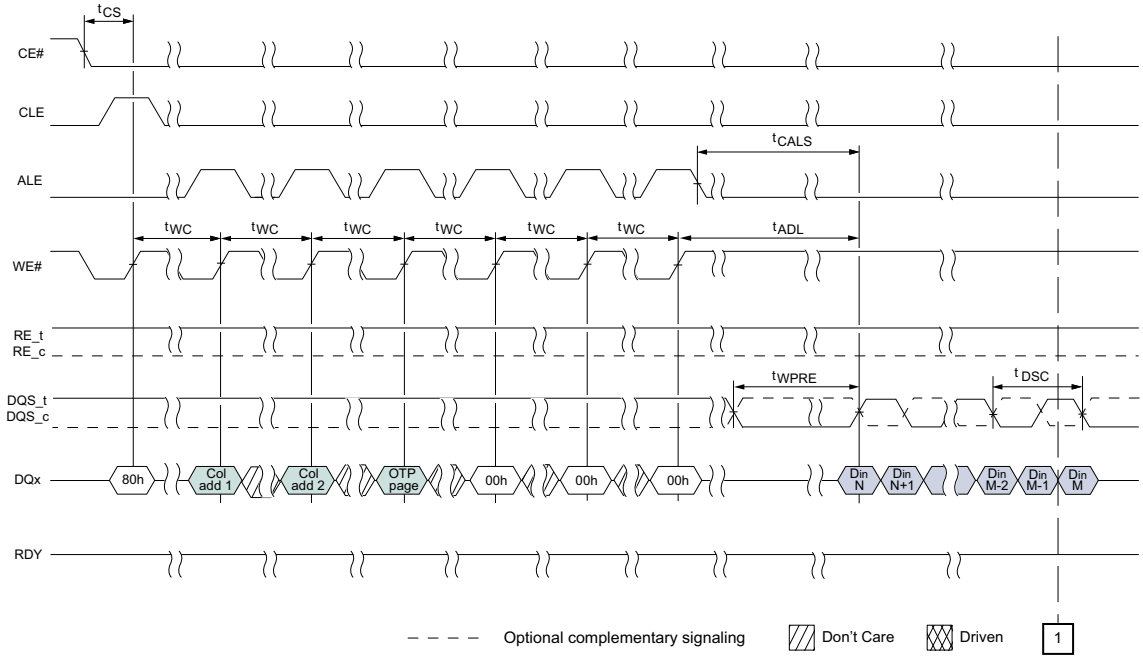
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 157: READ OTP PAGE



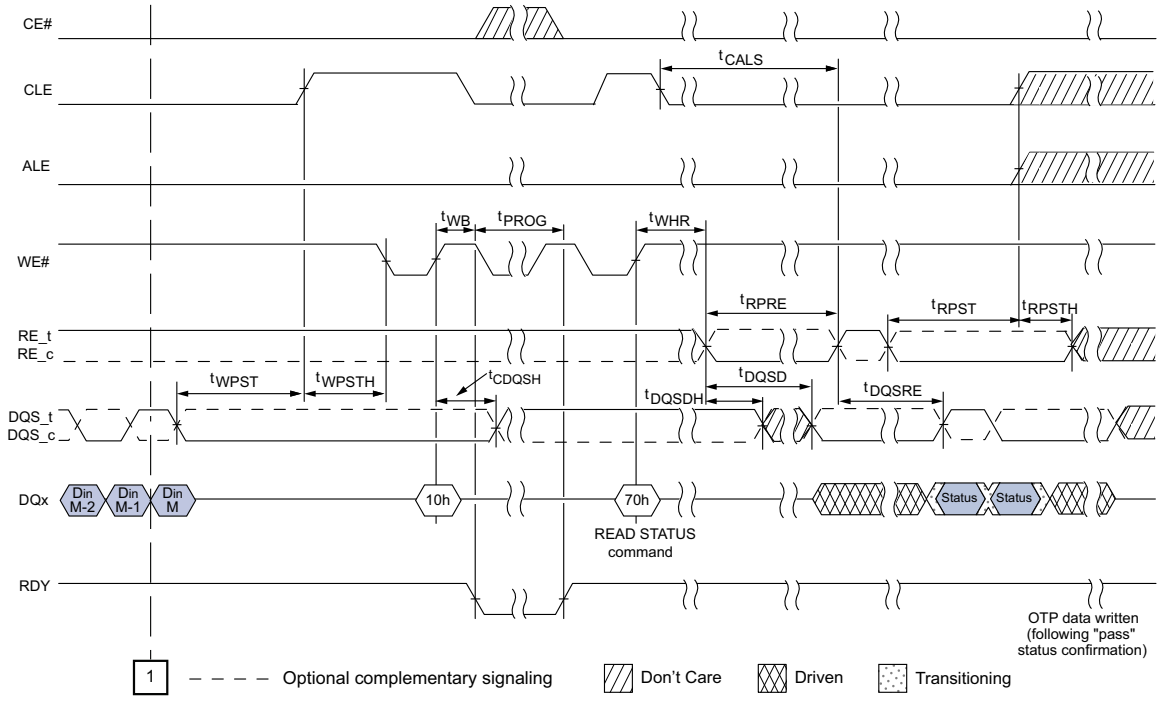
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 158: PROGRAM OTP PAGE (1 of 2)



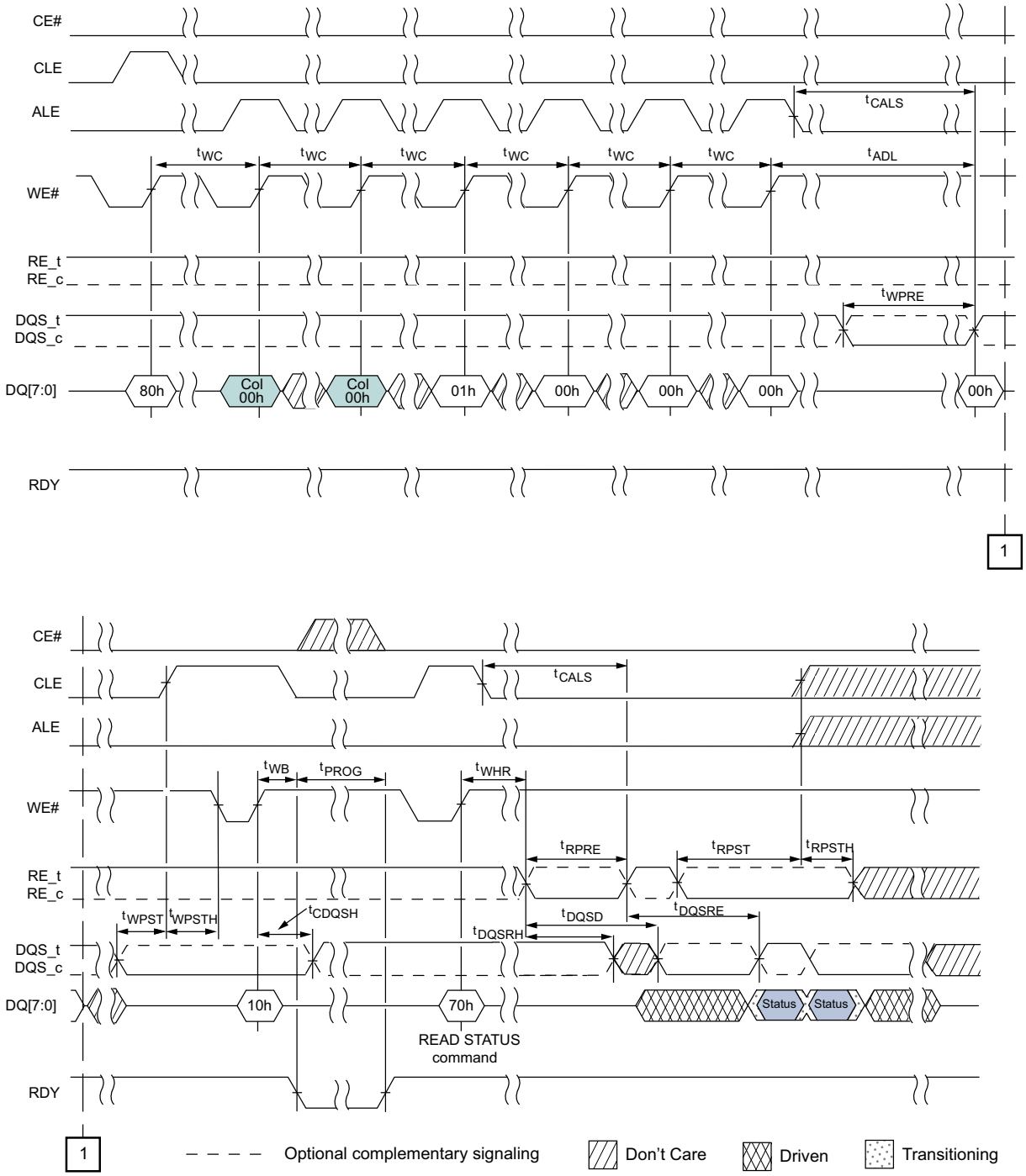
Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 159: PROGRAM OTP PAGE (2 of 2)



Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Figure 160: PROTECT OTP AREA



Note: 1. DQS is "Don't Care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Revision History

Rev. L – 08/26/21

- Under Electronic Mirroring section,
  - Added the sentence "The ODT CONFIGURE (E2h) command requires special handling for LUNs operating in mirrored DQ[7:0] mode. Refer to the ODT CONFIGURE (E2h) section."
- Under Command Definitions section,
  - Added "Read Assist Features" table
- Under Read Operations section,
  - Under READ PARAMETER PAGE (ECh) subsection,
    - In the first paragraph, changed “This command is accepted by the target only when all die (LUNs) on the target are idle.” to “This command shall be issued only when all LUNs are idle.”
    - Added paragraph: "All data from READ PARAMETER PAGE must be output before issuing any command other than READ STATUS (70h), which requires READ MODE (00h) or CHANGE READ COLUMN (05h-E0h) command to re-enable data output. If data output is interrupted, the READ PARAMETER PAGE (ECh) command needs to be reissued to the NAND."
  - Under READ UNIQUE ID (EDh) subsection,
    - In the first paragraph, changed “This command is accepted by the target only when all die (LUNs) on the target are idle.” to “This command shall be issued only when all LUNs are idle.”
    - Added paragraph: "All data from READ PARAMETER PAGE must be output before issuing any command other than READ STATUS (70h), which requires READ MODE (00h) or CHANGE READ COLUMN (05h-E0h) command to re-enable data output. If data output is interrupted, the READ UNIQUE ID (EDh) command needs to be reissued to the NAND."
- Under Configuration Operations section,
  - Under SET FEATURES (EFh) subsection,
    - In the first paragraph, changed “This command is accepted by the target only when all die (LUNs) on the target are idle.” to “This command shall be issued only when all LUNs are idle.
  - Under Feature Address 87h: Sleep Lite,
    - To the paragraph that starts with "Because LUNs in Sleep Lite mode cannot ...", added the sentences "high for tCEH. After the CE# signal is pulled HIGH for tCEH time, CE# is reasserted and all LUNs on a target revert to active states. The LUNs exiting Sleep Lite are required to meet the timing parameter specifications for CE# high > 1us even if CE# has not been high for > 1us (e.g. tCR2 and tCD)."
  - Under Feature Address DAh: Thermal Alert subsection,
    - Updated instances of "RDY (SR[6]) = 1" to "RDY (SR[6]) = 1 and ARDY (SR[5]) = 1 or 0"
    - Updated the thermal alert accuracy sentence from "The temperature readout is targeted to an accuracy of ±4ºC between the temperatures of 70ºC to 25ºC and an accuracy of equal to or less than ±8°C between the temperatures of 25°C to 0°C." to "The temperature readout is targeted to an accuracy of ±5ºC between the temperatures of 70ºC to 0ºC."
  - Under NAND operations and Thermal alert table, updated footnote sentence "SR[4], ESR[1], and ESR[0] bits will be invalid for Thermal Alert before RDY/ARDY (SR[6]/SR[5]) go high." to "SR[4], ESR[1], and ESR[0] bits will be invalid for Thermal Alert before RDY (SR[6]) goes high." pg122
  - Under Feature Address E7h: Temperature Sensor Readout,
    - Updated the Temperature sensor readout accuracy sentence from "The temperature readout is targeted to an accuracy of ±4ºC between the temperatures of 70ºC to 25ºC and an accuracy of equal to or less than ±8°C between the temperatures of 25°C to 0°C." to "The temperature readout is targeted to an accuracy of ±5ºC between the temperatures of 70ºC to 0ºC."
    - Under Temperature Sensor Readout parameter table, updated Max to 35 uS

  - Under ODT CONFIGURE (E2h) subsection,
    - Added “ODT CONFIGURE (E2h) for LUNs operating in mirrored mode” subsection.
- Under Status Operation section,
  - Changed occurrences for "RDY=1" to "RDY=1 and ARDY=1 or 0”
  - Under Status Register (SR) Definition table,
    - Under "SR Bit 4" definition, updated second to last sentence to "This bit is valid only when RDY (SR[6]) = 1 and ARDY (SR[5]) = 1 or 0."
- Under Read Operations section,
  - Added tRTABSY table "Read operations with tR reduction functionality"
  - Under CHANGE ROW ADDRESS (85h) subsection,
    - In the last paragraph, the sentence "The host can re-enable data output by issuing the 11h command, waiting tDBSY, and then issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command." to include 00h-05h-E0h for CHANGE READ COLUMN ENHANCED
  - Under Table Only Valid Commands when die (LUN) is Ready (RDY = 1, ARDY = 0) for READ PAGE (00h-30h), READ PAGE CACHE-series (31h, 00h-31h, 3Fh), and READ PAGE MULTI-PLANE (00h-32h),
    - Added rows for READ OFFSET PREFIX (2Eh) and SLC MODE LUN ENABLE (3Bh) VALID for every combination.
- Under TLC One Pass Programming section,
  - Under MLC Single Pass Programming Operations header,
    - In the second paragraph, added after the first sentence: "A PROGRAM PAGE (80h-10h) command sequence is only allowed to be issued to a die (LUN) when its RDY = 1 and ARDY =1."
    - For the paragraph that starts with "The PROGRAM PAGE MULTI-PLANE (80h-11h) command", added "A PROGRAM PAGE MULTI-PLANE (80h-11h) command is allowed when RDY = 1 and ARDY = 0 during program cache operations. Otherwise, a PROGRAM PAGE MULTI-PLANE (80h-11h) command is only allowed to be issued to a die (LUN) when its RDY = 1 and ARDY =1."
  - Under PROGRAM PAGE (80h-10h) subsection,
    - Updated instances of "RDY = 1" to "RDY = 1 and ARDY = 1"
  - Under PROGRAM PAGE MULTI-PLANE (80h-11h) subsection,
    - For instances of "(RDY =1)" updated to “(RDY =1, ARDY =1 for non-cache programming operations and RDY=1, ARDY=1 or 0 during cache programming)”
    - For Example command sequence for PROGRAM PAGE MULTI-PLANE (80h-11h) combined with PROGRAM PAGE CACHE (80h-15h) (End) - TLC One Pass (2-Planes), corrected steps 16 and 20 from tPBSY to tCBSY
  - Under PROGRAM SUSPEND (84h) and PROGRAM RESUME (13h) subsection,
    - Updated description for tRSPSPD to: "The LUN shall make forward progress for the program prior to suspending provided the delay from the PROGRAM RESUME (13h) to the subsequent PROGRAM SUSPEND (84h) command is longer than tRSPSPD. Note that tRSPSPD is defined as the minimum time required for EVERY program pulse to make forward progress regardless of the number of pulses allowed/required. Issuing a PROGRAM SUSPEND (84h) command after a PROGRAM RESUME (13h) with a delay shorter than tRSPSPD is not recommended but is allowed, but there may not be forward progress in the suspended program operation. Regardless of forward progress, a single program operation may not be suspended more than 30 times. If a delay is used which is shorter than tRSPSPD it cannot be guaranteed that the program operation will complete before reaching the maximum allowed suspend operations, and if the maximum allowed number of suspends is reached then the full remaining tPROG time must be allowed to complete without any further suspend operations."

    - Removed the paragraph: "While a program is suspended on a LUN, if host issues a program (80h-10h, 80h-15h, 85h-10h) based command or erase command (regardless of the address) to the suspended LUN, the program or erase command is not accepted by the LUN (R/B# goes LOW for tPSPDN) the LOCK status (SR[7] = 0) is set and the program that was suspended keeps its suspend state and can still be resumed. If a program or erase command is issued to a different LUN on the shared target then the program or erase is performed on the selected page or block and the program that was suspended keeps its suspend state."

  - Under Feature Address 7Fh: Manual Dynamic Word Line Start Voltage subsection,
    - Under Feature Address 7Fh: Manual Dynamic Word Line Start Voltage table, updated footnote 4 from "P1 value takes precedence over P3 value for a new block program when switching between blocks" to "If Feature Address 7Fh Sub-Feature P1 is set before a new block program, P1 value takes precedence over P3 value for a new block program when switching between blocks."
- Under Erase Operations section,
  - Under ERASE SUSPEND (61h) and ERASE RESUME (D2h) subsection,
    - Updated description for tRSESPD to: "The LUN shall make forward progress for the erase prior to suspending (e.g. complete an erase pulse) provided the delay from the ERASE RESUME (D2h) to the subsequent ERASE SUSPEND (61h) command is longer than tRSESPD. Note that tRSESPD is defined as the minimum time required for EVERY erase pulse to make forward progress regardless of the number of pulses allowed/required. Issuing an ERASE SUSPEND (61h) command after an ERASE RESUME (D2h) with a delay shorter than tRSESPD is not recommended but is allowed, but there may not be forward progress in the suspended erase operation. Regardless of forward progress, a single erase operation may not be suspended more than 30 times (i.e. it is allowed for a mix of delays longer and shorter than tRSESPD. If a delay is used which is shorter than tRSESPD it cannot be guaranteed that the erase operation will complete before reaching the maximum allowed suspend operations, and if the maximum allowed number of suspends is reached then the full remaining tBERS time must be allowed to complete without any further suspend operations."
- Under One-Time Programmable (OTP) Operations section,
  - Under Programming OTP Pages header,
    - Update second paragraph from "If the host issues a PAGE PROGRAM (80h-10h) command to an address beyond the maximum page-address range, the target will be busy for tOBSY and the WP# status register bit will be 0, meaning that the page is write-protected." to "It is illegal to issue any program command to an address outside the valid page-address range."
  - Under PROGRAM OTP PAGE (80h-10h) sub-section
    - Corrected tCCS for write depiction in PROGRAM OTP PAGE (80h-10h) with CHANGE WRITE COLUMN (85h) Operation
  - Under READ OTP PAGE (00h-30h) subsection,
    - Added paragraph: "All data from READ OTP PAGE must be output before issuing any command other than READ STATUS (70h), which requires CHANGE READ COLUMN (05h-E0h) command to re-enable data output. If data output is interrupted, the READ OTP PAGE (00h-30h) command needs to be reissued to the NAND."
    - Updated Figure READ OTP PAGE (00h-30h) Operation

- Under Error Management section,
  - Added paragraph:"While building a bad block table, or if the host has not determined if a block is a Factory Bad Block, or thereafter when accessing a Factory Bad Block, the only commands allowed are: SLC MODE LUN ENABLE (3Bh), READ PAGE (00h-30h), READ PAGE CACHE SEQUENTIAL (31h), READ PAGE CACHE RANDOM (00h-31h), READ PAGE CACHE LAST (3Fh), and READ PAGE MULTI-PLANE (00h-32h). Read assist features from the Read Assist Feature Table are not supported when the addressed block is a Factory Bad Block."
  - Updated External Data Randomization subsection.

- Under Electrical Specifications – DC Characteristics and Operating Conditions (NVDDR3) section,
  - Under 'DC Characteristics and Operating Conditions (NV-DDR3 Interface) 1.2V VCCQ' table
    - Updated SLC IWL ICC1_S (without/with vpp) Max. Avg. to 45/30 mA
    - Updated SLC IWLx2 ICC1_S (without/with vpp) Max. Avg. to 61/34 mA
    - Updated SLC Read ICC1_S (without/with vpp) Max. Avg. to 45/30 mA
    - Updated TLC IWL ICC1_S (without/with vpp) Max. Avg. to 38/28 mA
    - Updated TLC IWLx2 ICC1_S (without/with vpp) Max. Avg. to 44/29 mA
    - Updated TLC Read ICC1_S (without/with vpp) Max. Avg. to 58/42 mA
    - Updated SLC ICC2_S (without/with vpp) Max. Avg. to 61/41 mA
    - Updated TLC ICC2_S (without/with vpp) Max. Avg. to 63/41 mA
    - Updated SLC IWL ICC1_S (without/with vpp) Max. S.O. from 45/25 mA to 45/30 mA
    - Updated SLC IWLx2 ICC1_S (without/with vpp) Max. S.O. to 61/34 mA
    - Updated SLC Read ICC1_S (without/with vpp) Max. S.O. from 54/33 mA to 45/30 mA
    - Updated TLC IWL ICC1_S (without/with vpp) Max. S.O. from 38/25 mA to 38/28 mA
    - Updated TLC IWLx2 ICC1_S (without/with vpp) Max. S.O. to 44/29 mA
    - Updated TLC Read ICC1_S (without/with vpp) Max. S.O. 51/36 mA to 58/42 mA
    - Updated SLC ICC2_S (without/with vpp) Max. S.O. from 47/30 mA to 61/41 mA
    - Updated TLC ICC2_S (without/with vpp) Max. S.O. from 54/36 mA to 63/41 mA
    - Updated ICC3_S (without/with vpp) Max. from 38/32 mA to 38/36 mA
    - Updated ICC6_S Max. from 2 mA to 26 mA
    - Removed ICC4R_S, ICCQ4R_S, ICC4W_S, and ICCQ4W_S parameters from the table.
    - Added new table 'DC Characteristics and Operating Conditions (NV-DDR3 Interface) 1.2V VCCQ for Die (LUN) count per CE#' with ICC4R_S, ICCQ4R_S, ICC4W_S, and ICCQ4W_S parameters.
- Under AC Characteristics: NV-DDR3 Command, Address, and Data for Timing Modes 11-15 table,
  - Under Mode 13 - 15, changed tDQDQ spec max from 0.150ns to 0.200ns
- Under Electrical Specifications – Array Characteristics section,
  - Under TLC Array Characteristics table,
    - Updated tR (Max) from 63 µs to 67 µs
    - Updated tRSNAP (Max) from 56 µs to 59 µs
    - Updated tRCBSY2 (Max) from 63 µs to 67 µs
  - Under SLC Array Characteristics table,
    - Updated tR (Max) from 31 µs to 36 µs
    - Updated tRCBSY2 (Max) from 30 µs to 36 µs
    - Updated footnote 5 for OTP program from Xµs to 920 µs
- Under NV-DDR3 Interface Timing Diagrams section,
  - Updated READ PAGE CACHE SEQUENTIAL (1 of 2) figure to fix tRHW

Rev. K – 3/10/21

- Under B47R FortisFlash™ Features,
  - Under TLC Array Performance header,
    - Updated IWL READ operation time: 47us (TYP) from 45us (TYP)
- Under Status Operations section,
  - For the paragraph that starts with "SR[4] is the Status Register Flag Bit...",
    - Added 71h to the sentence "The Status Register flag bit SR[4] can be detected by the host with READ STATUS (70h), READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command."

    - Added the sentence "Any READ STATUS command (70h/78h/71h) should be issued before the next command so as not to lose Status Register Flag Bit SR[4] bit information since it gets reset every time RDY(SR[6]) goes LOW."

- Under Status Operations, under Status Register (SR) Definition table,
  - For SR Bit 4, ESR Flag bit, added sentence to the description: "During array operations, SR[4]=1 can indicate Vcc min violation, but SR[4]=0 does not indicate the absence of Vcc min violation"
  - Added the following statements to the note for SR[6] RDY and SR[5] ARDY: "A status value of ARDY =1 and RDY = 0 may occur as a result of the transition of status signals to other values (ie. ARDY transitions to a '1' faster than RDY transitions to a '1' or RDY transitions to a '0' faster than ARDY transitions to a '0'), but the ARDY = 1 and RDY = 0 status is a transitory value and therefore invalid and shall be ignored by the host. ARDY = 1 is only valid when RDY = 1."

- Under Status Operations section,
  - Under READ STATUS ENHANCED (78h) subsection, added paragraph "See the Interleaved Die (Multi-LUN) Operations section for data output requirements for interleaving operations between multiple die (LUNs)."
  - Under FIXED ADDRESS READ STATUS ENHANCED (71h) subsection, added paragraph "See the Interleaved Die (Multi-LUN) Operations section for data output requirements for interleaving operations between multiple die (LUNs)."

- Under Column Address Operations section,
  - Under CHANGE READ COLUMN ENHANCED (00h-05h-E0h) sub-section
    - Corrected tCCS for read depiction in figure
  - Under CHANGE WRITE COLUMN (85h) Operation
    - Corrected tCCS for read depiction in figure
  - Under CHANGE ROW ADDRESS (85h) sub-sections
    - Corrected tCCS for read depiction in figure
- Under Read Operations section, under Read Offset Prefix (2Eh) Command subsection, under Read Offset Prefix Restrictions heading,
  - Added new heading 'Interaction with READ PAGE CACHE SEQUENTIAL (31h)' with statement of "Read Prefix Offsets are not used or stored when a READ PAGE CACHE SEQUENTIAL (31h) command is issued to the last block, last page of a NAND plane as the page address is not re-read."
- Under TLC One Pass Programming Section,
  - Under PROGRAM SUSPEND (84h) and PROGRAM RESUME (13h) subsection,
    - Added paragraph at the end of the section: "During cache program, if a PROGRAM SUSPEND (84h) is issued, SR[4] is invalid until PROGRAM RESUME (13h) is issued. Thermal alert status may be monitored directly using the EXTENDED STATUS REGISTER READ (79h) command."
  - Under Feature Address 7Fh: Manual Dynamic Word Line Start Voltage subsection,
    - Added sentence to describe state after a reset operation: "Feature Address 7Fh sub-feature parameter output after a GET FEATURES by LUN (D4h) command will be P1=FFh, P2=P3=P4=00h."
- Under Erase Operations section, ERASE SUSPEND (61h) and ERASE RESUME (D2h) subsection,
  - Updated fourth paragraph which starts with "To suspend a ongoing erase operation to a LUN...", to indicate which bits are used for ERASE SUSPEND (61h)
    - Updated sentence from "the page address is ignored."
    - to "the block and page addresses are ignored. Only the LUN address is used for erase suspend."

- Under Restrictions During Suspend State section, Restrictions During Suspend State table,
  - Added row for CHANGE WRITE COLUMN (85h)

  - Updated row for PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), PROGRAM PAGE CACHE MULTI-PLANE (80h-15h), to include 85h on all instances

- Under TLC One Pass Copyback Operations section,
  - Under COPYBACK PROGRAM (85h-10h) sub-section,
    - Corrected tCCS for write depiction in COPYBACK PROGRAM (85h-10) with CHANGE WRITE COLUMN (85h) Operation - TLC One Pass figure
- Under One-Time Programmable (OTP) Operations section,
  - Under PROGRAM OTP PAGE (80h-10h) sub-section
    - Corrected tCCS for write depiction in PROGRAM OTP PAGE (80h-10h) with CHANGE WRITE COLUMN (85h) Operation
- Under Error Management section, Error Management Details table, clarified statement for Minimum required ECC "1e-2 RBER for TLC and 3.25e-3 RBER for SLC/SLC pages"
- Under Electrical Specifications – DC Characteristics and Operating Conditions (NV-DDR3) section,
  - Under DC Characteristics and Operating Conditions (NV-DDR3 Interface) 1.2V VCCQ table,
    - Added Max Single Operation values for ICC1_S, ICC2_S, ICC3_S, IPPA1, IPPA2, and IPPA3
- Under Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR3) section,
  - Under AC Characteristics: NV-DDR3 Command, Address, and Data for Modes 0–4 table,
    - Under Command and Address header, updated tAC description to "Access window of DQ[7:0] from RE# or RE_t/RE_c"
    - Under Data Output header, updated tAC description to "Access window of DQ[7:0] from RE# or RE_t/RE_c"
  - Under AC Characteristics: NV-DDR3 Command, Address, and Data for Modes 5–7 table,
    - Under Command and Address header, updated tAC description to "Access window of DQ[7:0] from RE# or RE_t/RE_c"
    - Under Data Output header, updated tAC description to "Access window of DQ[7:0] from RE# or RE_t/RE_c"
  - Under AC Characteristics: NV-DDR3 Command, Address, and Data for Modes 8–10 table,
    - Under Command and Address header, updated tAC description to "Access window of DQ[7:0] from RE# or RE_t/RE_c"
    - Under Data Output header, updated tAC description to "Access window of DQ[7:0] from RE# or RE_t/RE_c"
  - Under AC Characteristics: NV-DDR3 Command, Address, and Data for Modes 11–15 table,
    - Under Command and Address header, updated tAC description to "Access window of DQ[7:0] from RE# or RE_t/RE_c"
    - Under Data Output header, updated tAC description to "Access window of DQ[7:0] from RE# or RE_t/RE_c"
- Under Electrical Specifications section – Array Characteristics,
  - Under TLC Array Characteristics table,
    - Updated the description for ^{t}PROG to "PROGRAM PAGE operation time for Multi-Plane Program operations"
    - Updated the description for ^{t}PROG_eff to "Effective PROGRAM PAGE operation time for Multi-Plane Program operations"
    - Added a row for ^{t}PROG_SP with the description "PROGRAM PAGE operation time for Single-Plane Program operations" and value 2820 µs (Max)

  - Added a row for tPROG_SP_eff with the description "Effective PROGRAM PAGE operation time for Single-Plane Program operations" and value 650 µs (Typ)
  - Updated tRSNAP operation time from 45us (Typ) to 47us (Typ)
  - Updated tRTABSY time from 9.1us (Max) to 10us (Max)
  - Updated tRTABSY_IWL time from 6.4us (Max) to 6.8us (Max)
- Under SLC Array Characteristics table,
  - Updated tR operation time (Typ/Max) from 29/30us to 30uS/31us
  - Updated tRSNAP operation time (Typ/Max) from 26/27us to 24uS/26us
  - Updated tRTABSY time from 9.1us (Max) to 10us (Max)
  - Updated tRTABSY_IWL time from 6.4us (Max) to 6.8us (Max)

Rev. J – 12/23/20

- Under Features section,
  - Updated READ PAGE operation time: to 52us (TYP) from 56us (TYP)
  - Updated Effective Program page time: to 500us (TYP) from 502us (TYP)
  - Updated Erase block time: to 5ms (TYP) from 8ms (TYP)
  - Updated SLC Endurance to 60,000 PROGRAM/ERASE cycles from 80,000 PROGRAM/ERASE cycles
- Under Device Initialization section,
  - Under When Ramping V_{CC} and V_{CCQ}, under Ramp V_{CCQ} step 1.
    - Added the following,
- CE# and WE# should be ramped with V_{CCQ} during power-up and remain high at least 100µs after both V_{CC} and V_{CCQ} reach a stable voltage
- ALE and CLE should be low during V_{CCQ} ramp and remain low at least 100µs after both V_{CC} and V_{CCQ} reach a stable voltage
  - Updated R/B# Power-On Behavior figure,
    - Changed title to "Power-On Behavior figure"
    - Added CE#, CLE, ALE, and WE# signals to figure
- Under Electronic Mirroring section,
  - Updated the third and fourth paragraphs to: "The mirror and non-mirrored packages ..." and "The READ STATUS (70h) command is used to set devices...". Removed the fifth paragraph since it was combined with the fourth paragraph.
  - Removed reference to ENi and ENo in 132-Ball BGA Package in Mirrored DQ[7:0] Pinout figure
- Under TLC One Pass Programming section, under PROGRAM SUSPEND (84h) and PROGRAM RESUME (13h) subsection,
  - Removed Cache Read (00h-31h, 31h, 3Fh) commands from following statement "While a program is suspended, if host issues a Read (00h-20h, 00h-30h, 00h-35h) based command to the page address (or shared pages) of the suspended program the read will be performed with data output being undefined and the program that was suspended keeps its suspend state."
- Under Error Management section,
  - Under Error Management Details table, updated Minimum required ECC to add in SLC requirement: "TLC and SLC: LDPC to correct 1e-2 RBER and 3.25e-3 RBER for SLC/SLC pages"
  - Updated External Data Randomization subsection
- Under Electrical Specifications - DC Characteristics and Operating Conditions (NV-DDR3) section,

  - Updated I_{CC1}, I_{CC2}, I_{CC3}, I_{CC6}, I_{PPA1}, I_{PPA2}, and I_{PPA3} values.
- Under Electrical Specifications - AC Characteristics and Operating Conditions (NV-DDR3) section,
  - Under AC Characteristics: NV-DDR3 Command, Address, and Data for timing modes 11-15
    - Added dQSQ/dT and dQSQ/dV specifications for Timing Modes 13, 14 and 15 and accompanying note that they are not tested in production but guaranteed by design and characterization
    - Changed ^{t}QH for Timing Modes 13, 14, and 15 to "Not applicable"
    - Changed^{t}DQSQ for Timing Modes 13,14, and 15 to min = -0.150ns and max = 0.250ns
    - Added ^{t}DQDQ spec for Timing Modes 13, 14, and 15 with a max value of 0.150ns
    - Added note for^{t}DQSQ and ^{t}DQDQ "The ^{t}DQSQ is the worst case data output skew between DQS and DQ pins on a LUN while ^{t}DQDQ is the worst case data output skew between DQ pins on a LUN. The ^{t}DQDQ of a LUN however shall not cause ^{t}DQSQ to extend beyond the minimum and maximum ^{t}DQSQ specifications.
    - Changed ^{t}DQS2DQ for Timing Modes 11, 12, 13, 14, and 15 to min = -0.200ns and max = 0.200ns
    - Changed DQ2DQ for Timing Modes 11, 12, 13, 14, and 15 to max = 0.100ns

- Under Electrical Specifications - Array Characterization section,
  - Under TLC Array Characteristics table,
    - Updated the following spec values ^{t}PROG Typ and Max, ^{t}BERS Typ and Max, ^{t}R Typ and Max, ^{t}CBSY Typ and Max, ^{t}R_SBSBR Typ and Max, ^{t}RARC Typ and Max, ^{t}RCBSY1 Typ and Max, ^{t}RCBSY2 Typ and Max, ^{t}RSNAP Typ and Max, ^{t}RTABSY Typ and Max, ^{t}RTABSY_IWL Typ and Max.
    - Removed^{t}RST entry of "Reset during ^{t}PBSY time in a programming sequence
    - Added new ^{t}RST Read/Program/Erase note "After any array command, upon SR5/SR6 = 0, if a reset is issued, ^{t}RST will follow ^{t}RST (Program/Read/Erase). Array commands include all read operations/program operations/erase operations/copyback operations in the command set table. "
  - Under SLC Array Characteristics table,
    - Updated the following spec values ^{t}PROG Typ and Max, ^{t}BERS Typ and Max, ^{t}R Typ and Max, ^{t}CBSY Typ and Max, ^{t}RCBSY1 Typ and Max, ^{t}RCBSY2 Typ and Max, ^{t}RSNAP Typ and Max, ^{t}RTABSY Typ and Max, ^{t}RTABSY_IWL Typ and Max.

Rev. I – 11/20/20

- Under Features page,
  - Added note to NV-DDR3 I/O performance: "The I/O performance quoted only applies to NAND packages and channel topologies with up to 4 die per channel load. The 16-die 2-channel package only supports up to 1200 MT/s. The maximum data rate ... analysis."
- Under Bus Operation - NV-DDR3 Interface
  - Under NV-DDR3 Pausing Data Input/Output section
    - Changed section name to NV-DDR3 Pausing/Exiting/Interrupting Data Input/Output
    - 1st paragraph removed sentences: "The host will be required to exit the data burst if it wishes to disable ODT or re-issue warmup cycles when re-starting. If the host wishes to end the data burst, after exiting the data burst, a new command is issued."
    - 1st paragraph, 2nd sentence: changed phrase "The pausing of data output may be done by pausing …" to "The pausing of data output may also be done in the middle of a data output burst by …"
    - 1st paragraph, 3rd sentence: changed phrase "The pausing of data input may be done by pausing …" to "The pausing of data input may also be done in the middle of a data output burst by …"

- Added paragraph: "Pausing in the middle of a data input or data output burst is only allowed up to the 800MT/s data rate. Above 800MT/s, pausing in the middle of a data input or data output burst is not allowed, and if the data burst is interrupted, the host is required to exit first the data burst prior to resuming it."
- Added new paragraph "A data burst is exited when either ALE or CLE or CE# is toggled to a 1. After a data burst has been exited, if warmup cycles are enabled, then warmup cycles are required when re-starting the data burst. After a data burst has been exited, ODT also may be disabled, however if needed to meet the signal integrity needs of the system, ODT must be re-enabled prior to re-starting the data burst. If the host wishes to end the data burst, after exiting the data burst, a new command is issued."
- Added new paragraph "A data burst is interrupted when it is either paused or exited."
- Removed paragraph: "During the bus idle mode, all signals are enabled. No commands, addresses, or data are latched into the target; no data is output." as this same exact statement is already in the NV-DDR3 Idle section.
- Added paragraph: "The figure below is an example of exiting a data input burst with a CLE=1 and resuming the data input burst with a CLE=0. Warmup cycles if enabled are required to be issued when the data input burst is resumed." and added the "Data Input Burst Exit with CLE HIGH and Resume with CLE LOW" figure.
- Added paragraph: "The figure below is an example of exiting a data output burst with a CLE=1 and resuming the data output burst with a CLE=0. Warmup cycles if enabled are required to be issued when the data output burst is resumed." and added the "Data Output Burst Exit with CLE HIGH and Resume with CLE LOW" figure.
- Changed table title from "Data Input Sequence Pause and Resume Requirements if Data Input Sequence is Interrupted by CE# HIGH Pulse >1uS Duration" to "Data Input Sequence Interruption and Resume Requirements if Data Input Sequence is Interrupted by CE# HIGH Pulse >1uS Duration"
- Changed table title from "Data Output Sequence Pause and Resume Requirements if Data Output Sequence is Interrupted by CE# HIGH Pulse >1uS Duration" to "Data Output Sequence Interruption and Resume Requirements if Data Output Sequence is Interrupted by CE# HIGH Pulse >1uS Duration"
- Changed figure title from: "Data Input Burst Pause and Resume with CE# HIGH >1uS" to "Data Input Burst Interruption and Resume with CE# HIGH >1uS"
- Changed figure title from: "Data Output Burst Pause and Resume with CE# HIGH >1uS" to "Data Output Burst Interruption and Resume with CE# HIGH >1uS

- Under Identification Operations section,
  - Under Parameter Page Data Structure Table subsection
    - Under ONFI Parameter Page Data Structure table,
- Change Byte 195 and Byte 196 description from "Reserved" to "Plane Select LSB Bit Position in the Row Address Field". Change Byte 195 value to 0Ch and keep Byte 196 value at 00h
- Change Byte 113 description from "Number of interleaved address bits" to "Number of Bits to Address the Number of Planes in the Device". Change Bit[3:0] description from "Number of interleaved address bits" to "Number of Plane Select Bits"
- Update Integrity CRC Bytes 254 and 255

    - Under JEDEC Parameter Page Data Structure table,
    - Update Byte 8 -10 Description, update "Bit 10: 0 = supports Synchronous Reset" to "Bit 10: 1 = supports Synchronous Reset"

- Under Configuration Operations section,
  - Under SET FEATURES (EFh) subsection,

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    - In 4th paragraph, replaced text: "The READ STATUS (70h) command can be used to monitor for command completion. During ^{t}FEAT, it is prohibited to issue READ STATUS ENHANCED (78h) command." with "For 1 LUN per target ... issuing the next command."
    - Added paragraph: "Use of READ STATUS (70h/71h/78h) ..."
  - Under GET FEATURES (EEh) subsection,
    - In 3rd paragraph, replaced text: "If the READ STATUS (70h) command is used to monitor ... use of the READ STATUS ENHANCED (78h) command is prohibited." with "For 1 LUN per target ... See the GET/SET FEATURES by LUN (D4h/D5h) section for details."
  - Under Feature Address 84h: Clear Extended Status Register, added "Clear" to tile of table.
  - Under Feature Address 86h: Read Offset Values Reset subsection:
    - Updated Feature Address 86h table.
    - Updated second paragraph to: "The Read Prefix Offsets can be reset with Feature Address 86h by setting Subfeatures P1-P4 to 00h. It will take ^{t}FEAT2 time to fully reset all the read offsets."
- Under Status Operations section,
  - In Status Register (SR) Definition table:
    - Updated bit 4 definition to: "ESR Flag Bit: Low VCC Alert/Thermal Alert High or Low" and description to: "ESR Flag Bit 0 = default, 1 = Error event from ESR[7:0] or Power-on default. The NAND will set the SR bit 4, when VCC min is violated during an ongoing Read, Program, or Erase operation (e.g. SR[5] = 0), or a Thermal Alert Status Temperature is outside (low or high) the defined temperature range after valid NAND array operation. This bit is valid only when ARDY (SR[5]) or RDY (SR[6]) is 1. Power-on default for SR[4] = 1."
  - In Extended Status Register (ESR) Definition table:
    - Added definition for bit 3: "Low VCC Alert" with the description: "Status = 0: default, Status = 1: The NAND will set ESR[3] when VCC is lower than VCC min during an ongoing Read, Program, or Erase operation (e.g. SR[5] = 0). This bit is persistent and must be cleared using Feature Address 84h: Clear Extended Status Register.".
    - Under ESR Bit 3, 1, and 0: Added "Clear" to description of Feature Address 84h: Clear Extended Status Register
- Under Read Operations section, under Read Offset Prefix Command (2Eh) subsection,
  - Under Read Prefix Offset Restrictions and Clearing Read Offsets topics updated "Feature Address 86h: P1[0] = 1" to "Feature Address 86h: P1-P4 = 00h"
- Under Feature Address A0h to ABh section
  - In 1st paragraph, update 'Feature Address 86h: P1[0] = 1" to "Feature Address 86h: P1-P4 = 00h"
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Rev. H – 09/30/20

- Under B47R FortisFlash™ Features section
  - Under Organization,
    - Update Plane size from 4 planes x 552 blocks to 4 planes x 556 blocks.
    - Update device size for 512Gb from 2208 blocks to 2224 blocks; 1Tb from 4416 blocks to 4448 blocks; 2Tb from 8832 blocks to 8896 blocks; 4Tb from 17,664 blocks to 17,792 blocks; and 8Tb from 35,328 blocks to 35,584 blocks
  - Update TLC Array Performance - Erase block time TYP from 5ms to 8ms.
- Under Device and Array Organization section,
  - Update Array Organization per Logical Unit (LUN) for B47R in TLC mode to reflect 2224 blocks per LUN from 2208 blocks per LUN

  - Under Array Addressing for Logical Unit (LUN) for B47R in TLC mode, update note 7 to reflect 2224 blocks per LUN from 2208 blocks per LUN
  - Update Array Organization per Logical Unit (LUN) for B47R in SLC mode to reflect 2224 blocks per LUN from 2208 blocks per LUN
  - Under Array Addressing for Logical Unit (LUN) for B47R in SLC mode, update note 7 to reflect 2224 blocks per LUN from 2208 blocks per LUN

- Under Volume Addressing section,
  - Under Volume Appointment subsection, Added sentence: "All LUNs on a CE# must have the same volume address."
- Under Data Training section, Under DCC Training subsection,
  - Removed 1st paragraph and replaced with "Explicit DCC training shall be performed after ZQ calibration is completed. Explicit DCC training shall be supported by NAND devices operating over 800 MT/s. Explicit DCC training can be enabled via Feature Address 20h: DCC Training and Write DQ Training (Tx side). Depending on the ODT Self-Termination usage on the CE#, Explicit DCC Training may be done one LUN at a time (Single LUN DCC Training) or in parallel (Parallel DCC Training).
  - Removed Explicit DCC Training sub-section
  - Added Single LUN DCC Training sub-section
    - Added verbiage with requirements and instructions on how to perform Single LUN DCC Training
    - Added figure showing how Single LUN DCC Training Using SET FEATURE by LUN (D5h) is done
  - Added Parallel LUN DCC Training sub-section
    - Added verbiage with requirements and instructions on how to perform Parallel LUN DCC Training
    - Added figure showing how Parallel LUN DCC Training Using SET FEATURE by LUN (D5h) is done
  - After Feature Address 20h table, added DCC Training Reset Behavior sub-section
- Under Identification Operations section, Under Parameter Page Data Structure Tables
  - Under ONFI Parameter Page Data Structure Table
    - Updated Byte 96 from A0h to B0h (Blocks per LUN)
    - Updated Byte 103 from 68h to 78h (Bad blocks maximum per LUN)
    - Update Bytes 135,136 from 30h, 75h to 20h, 4Eh (^{t}BERS Max
    - Updated Byte 193,194 from Bits[15:2]: Reserved (0) to Bits[15:3]: Reserved (0) and Bit[2] 1 = Factory Reserved Setting
    - Updated Byte 15394 from 68h to 78h (Bad blocks maximum per LUN)
  - Under JEDEC Parameter Page Definition Table
    - Updated Byte 96 from A0h to B0h (Blocks per LUN)
    - Update Bytes 155,156 from 30h, 75h to 20h, 4Eh (^{t}BERS Max)
    - Updated Byte 213 from 68h to 78h (Bad blocks maximum per LUN)
    - Updated Byte 438,439 from Bits[15:2]: Reserved (0) to Bits[15:3]: Reserved (0) and Bit[2] 1 = Factory Reserved Setting
- Under TLC One Pass Programming section, under PROGRAM SUSPEND (84h) and PROGRAM RESUME (13h) subsection,
  - Added statement "The host shall resume the operation by issuing PROGRAM RESUME (13h) within ^{t}SUSPEND_P of issuing PROGRAM SUSPEND (84h)." to first paragraph.

- Under Erase Operations section, under ERASE SUSPEND (61h) and ERASE RESUME (D2h) subsection,
  - Added statement "The host shall resume the operation by issuing ERASE RESUME (D2h) or ERASE BLOCK (60h-D0h) within ^{t}SUSPEND_E of issuing ERASE SUSPEND (61h)." to first paragraph.
- Under Nested Suspend section,
  - Added statement "When using Nested Suspend, the host shall follow the specifications: ^{t}SUSPEND_P for Program Suspend and ^{t}SUSPEND_E for Erase Suspend." to third paragraph.
- Under Restrictions During Suspend State section,
  - Updated operation names to reflect full datasheet name
  - Removed Note 5 from table
- Under Error Management section, under Error Management Details table,
  - Update total available blocks per LUN to 2224 from 2208
  - Under Minimum required ECC, changed SLC from "60-bit ECC per 1147 bytes of data" to "LDPC to correct 1e-2 RBER" and removed note 2
- Under Electrical Specifications section, Under Valid Blocks per LUN table, update Max to 2224 from 2208
- Under Electrical Specifications - AC Characteristics and Operating Conditions (NV-DDR3)
  - Added ^{t}CSVOL spec with min value of 100ns to all Timing Modes
  - Under AC Characteristics: NV-DDR3 Command, Address, and Data for timing modes 11 - 15 table
    - Changed ^{t}DVWd spec entries for Timing Modes 13, 14 and 15 from: "^{t}DVWd=^{t}QH-^{t}DQSQ" to "Not applicable. DCC Training and per-DQ Read Training are required for data rates >1200MT/s and the ^{t}DVWp spec shall be used."
    - Changed last sentence of the Note for ^{t}DVWp spec from: "^{t}DVWp (per pin valid window) applies only when DCC training is enabled for >800MT/s data rates " to "For >800MT/s data rates, use of the ^{t}DVWp (per pin valid window) spec requires that the system performs DCC training and per-DQ Read Training for each LUN"
- Under Electrical Specifications - Array Characteristics section,
  - Under TLC Array Characteristics Table
    - Update ^{t}BERS ERASE BLOCK operation time from 5ms to 8ms (Typ) and from 30ms to 20ms (Max)
    - Update ^{t}DBSY Typ spec from "0.5" to "-"
    - Added ^{t}SUSPEND_E and ^{t}SUSPEND_P specs to table and associated note: It is the host's responsibility to ensure that the time elapsed between the SUSPEND operation and the RESUME operation meets the corresponding ^{t}SUSPEND_P or ^{t}SUSPEND_E specification, or both of them in the case of Nested Suspend
  - Under SLC Array Characteristics Table
    - Update ^{t}BERS ERASE BLOCK operation time from 5ms to 8ms (Typ) and from 30ms to 20ms (Max)
    - Added ^{t}SUSPEND_E and ^{t}SUSPEND_P specs to table and associated note: It is the host's responsibility to ensure that the time elapsed between the SUSPEND operation and the RESUME operation meets the corresponding ^{t}SUSPEND_P or ^{t}SUSPEND_E specification, or both of them in the case of Nested Suspend

Rev. G – 07/30/20

- Under B47R FortisFlash™ Features section
  - Update TLC Array Performance - Erase block time from 15ms to 5ms.
  - Update SLC Endurance from 100,000 PROGRAM/ERASE cycles to 80,000
- Under Signal Assignments section, Under 132-ball BGA (Ball-Down, Top View) figure, update pin P1 and R1 from "R" to "DNU"
- Under Package Dimensions section,
  - Update 132-Ball Figures (Package Code: J4 and M4) Dimensions 132X Ø0.55 to 132X Ø0.551±0.05 and Ball to Package offset from 0.3 ±0.05 to 0.299 ±0.04
  - Update 132-Ball Figures (Package Code: M5) Ball to Package offset from 0.3 ±0.05 to 0.295 ±0.04
- Under Bus Operation - NV-DDR3 Interface section, under NV-DDR3 Pausing Data Input/Output subsection, under Data Output Sequence Pause and Resume Requirements if Data Output Sequence is Interrupted by a CE# HIGH Pulse >1uS Duration table, update instances of "^{t}RCBSY" to "^{t}RCBSY1 or ^{t}RCBSY2"
- Under Electronic Mirroring section, update figure to Example of 132-Ball BGA Package in Mirrored DQ[7:0] Pinout from 152-Ball Example.
- Under Read Operations section,
  - Under READ MODE (00h) section, added READ MODE (00h) figure
  - Update all instances of "^{t}RCBSY" to "^{t}RCBSY1 or ^{t}RCBSY2"
  - Updated READ PAGE CACHE SEQUENTIAL (31h) Operation, READ PAGE CACHE RANDOM (00h-31h) Operation, and RAD PAGE CACHE LAST (3Fh) Operation figures to separate ^{t}RCBSY into ^{t}RCBSY1 and ^{t}RCBSY2
  - Under Read Offset Prefix (2Eh) Command sub-section,
    - Updated ^{t}RTABSY to ^{t}RTABSY_IWL in following figures: Read Offset Prefix Command (2Eh) with IWL Read (00h-20h) with ACRR Enabled and IWL READ IWLx2 Offset Location
  - Under IWL READ (00h-20h) sub-section,
    - Updated ^{t}RTABSY to ^{t}RTABSY_IWL for the following figures: IWL Read (00h-20h) Operation, IWL Read (00h-20h) Operations with ACRR Enabled, FEATURE ADDRESS A0h-ABh Offsets for 2 Plane Group IWL, IWLx2 Timing Sequence for 00h-20h (1 of 2), and IWLx2 Timing Sequence for 00h-20h (2 of 2).
- Under TLC One Pass Programming section, under PROGRAM SUSPEND (84h) and PROGRAM RESUME (13h) subsection
  - Added new paragraph starting with "During SLC cache program, if PROGRAM SUSPEND (84h) is issued after PROGRAM PAGE CACHE (80h-15h)....."
  - Under Feature Address 7Fh: Manual Dynamic Word Line Start Voltage section, updated section to reflect current implementation
    - Updated "predetermined word line interval" to "first page of a wordline"
    - Update SLC/TLC paragraph with new header: DWLSV can be applied to both TLC and SLC blocks but not to SLC/MLC edge WLs in a TLC block.
    - Added new paragraph on SLC block operation
    - Update statement "FA=7Fh P1 still contains the last issued user offset." to "After programming of the page, the NAND will populate Sub-Feature P3 with the new sampled value (if user page is the first page of a wordline) or the Sub-Feature P1 value provided by the host. Feature Address 7Fh Sub Feature P1 will still contain the last issued user offset."

  - Update statement "If the WLSV offset information is not available, the default WLSV will be used." to " If the DWLSV offset information is not available, the default WLSV will be used and DWLSV sampling will happen on the first age that is programmed."
  - Updated notes to Feature Address 7Fh: Manual Dynamic Word Line Start Voltage table
  - Under note 2: Changed "Set Feature by LUN (D5h) value of 00h to FA=7Fh P1 will disable MDWLSV feature." to Set Feature by LUN (D5h) value of 00h to FA=7Fh P1 will cause a voltage offset of zero to be applied. A new MDWSLV voltage offset will be calculated on the next sample boundary.
  - Add to note 2: Set Feature by LUN (D5h) value of FEh to FA=7Fh P1 is a special value that will use zero offset for both page N and page N+1. A new MDWSLV voltage offset will be calculated on page N+1
  - Updated note: "Only the NAND generated offset values can be applied to FA=7Fh P1; otherwise, the operation cannot be guaranteed." with "Array reliability will not be guaranteed if the host inputs non-NAND generated values into Feature Address 7Fh P1[7:0]. If correct DSV information is unknown/lost, DO NOT load any value into Feature Address 7Fh P1[7:0]."

- Under One-Time Programmable (OTP) Operations section,
  - update statement in Programming OTP Pages from "Each page in the OTP area is programming using the PROGRAM OTP PAGE (80h-10h) command. Each page can be programmed more than once, in sections, up to the maximum number allowed (see NOP in the OTP Area Details table)." to "Each page in the OTP area is programmed using the PROGRAM OTP PAGE (80h-10h) command. Each page can only be programmed once (see NOP in the OTP Area Details table) and the host is not required to fill a page worth of data during the program command sequence."
  - OTP Area Details table: changed Number of partial page programs (NOP) to each OTP page from 2 to 1.

- Under Electrical Specifications section, in first paragraph update statement "Exposure to absolute maximum rating conditions for extended periods can affect reliability." to "Exposure to conditions above the recommended operating range or absolute maximum rating conditions for extended periods can affect reliability."
- Under Electrical Specifications - DC Characteristics and Operating Conditions (NV-DDR3) section,
  - Update Array read current (active) ICC1 values
  - Update V_{PP} current (active) I_{PPA1} and I_{PPA2}values
  - Updated I/O burst read and write current values for all speed ranges: ICC4R, ICCQ4R, ICC4W, and ICCQ4W

- Under Electrical Specifications - Array Characteristics section,
  - Under TLC Array Characteristics table,
    - Update Erase Block Operation Time ^{t}BERS Typ to 5ms from 15ms
    - Update Cache program operation time and PROGRAM PAGE operation time Max specs from 2259us to 2822us.
    - Update Page Buffer Transfer Busy time ^{t}PBSY Typ to 6us from 12us and Max to 10us from 14us.
    - Update Power-on reset time ^{t}POR Typ to 1.5ms from 2ms.
    - Split ^{t}RCBSY into ^{t}RCBSY1 for RDY/ARDY = 1, ^{t}RCBSY2 for RDY = 1, ARDY = 0 or 1. Set ^{t}RCBSY1 Max = TBD.
    - Split ^{t}RST Device reset time (Read/Program/Erase) into separate specs for each and added ^{t}RST (Erase) typical = 75us.
    - Split ^{t}RTABSY into ^{t}RTABSY for array read operation and ^{t}RTABSY_IWL for array IWL read operation

- Updated Parameter for tRTABSY from "Busy time in a non-cache read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH" to "Busy time for read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array read operation", updated value to 10us typ and 12us max
- Added note: tRTABSY applies to all array Read operations (excluding IWL). In Cache Read based operations tRTABSY still applies before the next array Cache Read operation begins.
- Added Parameter for tRTABSY_IWL of " Busy time for IWL read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array IWL read operation", with value of 6us typ and 10us max
- Added note: tRTABSY_IWL applies to all IWL Read operations.
- Update tZQCL and tZQCS values from Typ to Max values to reflect ONFI standards.
- Update note for Number of partial page programs from "The pages in the OTP Block have an NOP of 2." to "The pages in the TLC Block have an NOP of 1."

– Under SLC Array Characteristics table,

- Update Erase Block Operation Time tBERS Typ to 5ms from 15ms
- Under Number of partial page programs, update Max value from 2 to 1.
- Update Cache program operation time and PROGRAM PAGE operation time Max specs from 400us to 836us.
- Split tRCBSY into tRCBSY1 for RDY/ARDY = 1, tRCBSY2 for RDY = 1, ARDY = 0 or 1. Set tRCBSY1 Max = TBD.
- Split tRTABSY into tRTABSY for array read operation and tRTABSY_IWL for array IWL read operation
- Updated Parameter for tRTABSY from "Busy time in a non-cache read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH" to "Busy time for read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array read operation", updated value to 10us typ and 12us max
- Added note: tRTABSY applies to all array Read operations (excluding IWL). In Cache Read based operations tRTABSY still applies before the next array Cache Read operation begins.
- Added Parameter for tRTABSY_IWL of " Busy time for IWL read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array IWL read operation", with value of 6us typ and 10us max
- Added note: tRTABSY_IWL applies to all IWL Read operations.
- Update note for Number of partial page programs from "The pages in the OTP Block have an NOP of 2." to "The pages in the SLC Block have an NOP of 1."

- Under NV-DDR3 Interface Timing Diagrams section,
  – Update READ PAGE CACHE SEQUENTIAL and READ PAGE CACHE RANDOM figures to separate tRCBSY into tRCBSY1 and tRCBSY2

Rev. F – 06/30/20

- Under Device Initialization section,
  – Updated the first bullet of note 5 to: "Status can be checked using FIXED ADDRESS READ STATUS ENHANCED (71h). Checking status with READ STATUS (70h) or READ STATUS ENHANCED (78h) command is prohibited during tPOR."

- Under DCC Training section,
  - Under first paragraph, replaced "RANDOM DATA OUT (00h-05h-E0h)" with "CHANGE READ COLUMN ENHANCED (00h-05h-E0h)" and added the statement "CHANGE READ COLUMN ENHANCED (06H-E0h) is not supported."
- Under Configuration Operations section,
  - Updated Feature Address Definitions Table with 86h: Read Offset Values Reset
  - Added new Feature Address 86h: Read Offset Values Reset subsection.
  - Under Feature Address DAh: Thermal Alert subsection, removed statement "Status Register flag bit SR[4] remains set until a reset by a new algo with the following exceptions:" and removed list of exceptions.
- Under Status Operations section,
  - In fourth paragraph, removed statement "Status Register Flag Bit SR[4] remains set until a reset with a new algo corresponding to RDY (SR[6]) = 0 with the following exceptions:" and list of exceptions.
- Under Column Address Operations section,
  - Under CHANGE READ COLUMN (05h-E0h) subsection, changed statement "It is also accepted by the selected die (LUN) during CACHE READ operations (RDY = 1; ARDY = 0)." to "It is also accepted by the selected die (LUN) during CACHE operations (RDY = 1; ARDY = 0) but is limited to CACHE READ. CACHE PROGRAM is not allowed.
  - Under CHANGE READ COLUMN ENHANCED (06h-E0h) subsection, changed statement "This command is accepted by a die (LUN) when it is ready (RDY = 1; ARDY = 1)." to "This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE operations (RDY = 1; ARDY = 0) but is limited to CACHE READ. CACHE PROGRAM is not allowed.
- Under Read Offset Prefix (2Eh) Command section,
  - Under Read Offset Prefix Restrictions, updated statement "To clear the read offset values the host would have to issue the prefix command (2Eh) with all 00h offset values or issue a HARD RESET (FDh) command which will reset offset values to 00h." to "To clear the read offset values the host would have to issue the prefix command (2Eh) with all 00h offset values to each page type, issue a HARD RESET (FDh) command, or issue a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) to Feature Address 86h: P1[0] = 1 which will reset all stored Read Offset Prefix values to 00h."
  - Under Clearing Read Offsets, updated statement "To clear the read offset values the host would have to issue the prefix command (2Eh) with all 00h offset values or issue a HARD RESET (FDh) command which will reset offset values to 00h." to "To clear the read offset values the host would have to issue the prefix command (2Eh) with all 00h offset values to each page type, issue a HARD RESET (FDh) command, or issue a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) to Feature Address 86h: P1[0] = 1 which will reset all stored Read Offset Prefix values to 00h."
- Under Feature Address A0h-ABh section, in first paragraph updated wording "... after the host issued reset command after a power cycle." to "... after the host issued HARD RESET (FDh) command. Issuing a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) to Feature Address 86h: P1[0] = 1 will clear all previous stored Read Offset Prefix values stored in Feature Address A0h-ABh Subfeature P1 and P2 to 00h.
- Under Interleaved Die (Multi-LUN) Operations section,
  - In the paragraph: "When issuing combination of commands...", updated the last sentence to: "After the READ STATUS ENHANCED (78h) command is issued to the selected die (LUN) a CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (00h-05h-E0h / 06h-E0h) command shall be issued prior to any data output from the selected die (LUN).
- Under Electrical Specifications - Package Electrical Specifications and Pad Capacitance sub-section,
  - In LUN Pad Specification Table

  - Changed C_Pad$_{IO}$ Typ from "-" to 1.1pF and Max from TBD to 1.3pF
  - Changed C_Pad$_{ZQ}$ Typ from "-" to 1.0pF and Max from TBD to 1.84pF

- Under Electrical Specifications - Array Characteristics Section,
  - Under TLC Array Characteristics table,
    - Under Auto Read Calibration time, update ^{t}RARC Typ to 475us and ^{t}RARC max to 670us.
    - Under Cache program operation time, update ^{t}CBSY max to 2259us.
  - Under SLC Array Characteristics table,
    - Under Cache program operation time, update ^{t}CBSY max = 400us

Rev. E – 05/25/20

- Under Command Definitions section,
  - Added new paragraph at beginning of "Commands other than those defined in the Command Set table are illegal and shall not be issued to the NAND."
  - Added new note #1 to Command Set Table and linked to each command of "Commands other than those defined in the Command Set table are illegal and shall not be issued to the NAND."

- Under Identification Operations section, Under READ ID Parameter Tables
  - In Read ID Parameters for Address 00h and 20h, updated MT29F1T08EELDE to MT29F1T08EELEE
  - In Read ID Parameters for Address 00h and 20h, updated MT29F2T08EMLDE to MT29F2T08EMLEE

- Under Configurations Operations section, Under Feature Address Details subsection,
  - Under Feature Address 01h: Timing Mode, Updated Subfeature Parameter P1: Program Clear bit from "Program command clears all cache registers on a target (default)" to " Program command clears all cache registers on a target as long as the program command is issued when RDY=1 (default)"
- Under Read Operations section,
  - Removed header: "Reading and Clearing Read Offsets"
  - Added header: "Clearing Read Offsets" and new paragraph: "To clear the read offset values the host would have to issue the prefix command (2Eh) with all 00h offset values or issue a HARD RESET (FDh) command which will reset offset values to 00h. Other RESET commands will not clear the read offset values."

- Under TLC One Pass Programming section,
  - Under PROGRAM SUSPEND (84h) and PROGRAM RESUME (13h) subsection,
    - added statement to end of first paragraph: "When using program suspend, the observed ^{t}PROG may exceed ^{t}PROG (Max)."
    - Removed Feature Address list of allowed SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands permitted during program suspend and added link to new section "Restrictions During Suspend State"
    - In paragraph beginning with " While a program is suspended, if the host issues a RESET (FFh, FAh, FDh) command for the affected LUN, then the program that was suspended is canceled and status is cleared." added new statement "The ^{t}RST time that will elapse during this operation is ^{t}RST during program since it is actively cancelling a program suspend operation."
    - Added statement: "See Restrictions During Suspend State for Valid Operations during Program Suspend."

- Under Erase Operations section, under ERASE SUSPEND (61h) and ERASE RESUME (D2h) subsection,

  - In paragraph beginning with "While an erase is suspended, if the host issues a RESET....the status is cleared.", added new statement "The ^{t}RST time that will elapse during this operation is ^{t}RST during erase since it is actively cancelling an erase suspend operation."
  - Removed Valid Operations during Erase Suspend table and added statement with link to new section "Restrictions During Suspend State".

- Under Nested Suspend section,
  - Removed statement: "NAND is limited to certain operations after nested suspend (i.e. program suspend after erase suspend). Limitations are listed in PROGRAM SUSPEND (84h) section. The following table describes valid/invalid operations. Invalid operations do not have specific behavior expected from NAND except for certain scenarios mentioned in the table below. "
  - Removed Valid/Invalid Operations in Nested Suspend State table
  - Added statement and link "For Valid Operations during Nested Suspend, See Restrictions During Suspend State"
  - Added new paragraph: "While the NAND is in a nested suspend state, if the host issues a RESET (FFh, FAh, FDh) command for the affected LUN, then the suspended state is cancelled and status is cleared. The ^{t}RST time that will elapse during this operation is the maximum ^{t}RST between program and erase operations."

- Added new section: "Restrictions During Suspend State" to cover Program Suspend, Erase Suspend, and Nested Suspend.
- Under Electrical Specifications - Array Characteristics section,
  - In TLC Array Characteristics table, added new note for PROGRAM PAGE operation time: "When using program suspend, the observed total ^{t}PROG may exceed ^{t}PROG (Max)"
  - In SLC Array Characteristics table, added new note for PROGRAM PAGE operation time: "When using program suspend, the observed total ^{t}PROG may exceed ^{t}PROG (Max)"
  - In TLC Array Characteristics table for Power-on reset time, updated ^{t}POR Max to 4ms from 10ms.
  - Updated TLC Array Characteristics table and SLC Array Characteristics table TBD entries with values and updated ^{t}RCBSY typical, SLC ^{t}PROG Max, SLC ^{t}RSNAP values.

Rev. D – 04/10/20

- Under Device Features section,
  - Changed ONFI4.1 compliant to ONFI4.2 compliant.
  - Under Part Number Diagram, changed topic: "Reserved for Future Use" to "Special Options" with "R = FortisFlash™" and added R to the part number line.

- Under Device Initialization section,
  - Changed step 5 from "The RESET busy time tPOR can be monitored by polling R/B# or polling FIXED ADDRESS READ STATUS ENHANCED (71h) on each LUN." to " The RESET busy time tPOR can be monitored by polling R/B# or polling the status register of each LUN."
  - Changed Step 5 sub-bullet from "Checking status with READ STATUS (70h) or READ STATUS ENHANCED (78h) command is prohibited during tPOR. The host must not issue an additional RESET (FFh) command during tPOR." to
    - "Status can be checked using READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h). Checking status with READ STATUS (70h) command is prohibited during tPOR.
    - The host must not issue an additional RESET (FFh) command during tPOR."

- Under Volume Addressing section,
  - Under Selecting a Volume subsection,

  - Replaced "100ns" with "^{t}CSVOL"
- Under Identification Operations section
  - Under READ ID (90h) subsection,
    - Updated wording for Address 20h to: "When the 90h command is followed by a 20h address cycle, the target returns 6 bytes of data beginning with the 4-byte ONFI identifier code ('O'=4Fh, 'N'=4Eh, 'F'=46h, 'I'=49h)."
    - Updated wording for Address 40h to: " When the 90h command is followed by a 40h address cycle, the target returns 6 bytes of data beginning with the 5-byte JEDEC identifier code ('J'=4Ah, 'E'=45h, 'D'=44h, 'E'=45h, 'C'=43h.)."
    - Update figure READ ID (90h) with 40h Address Operation: Align ^{t}WHR with start of ^{D}OUT.
  - Under Parameter Page Data Structure Tables,
    - Under ONFI Parameter Page Data Structure table, updated the following bytes
  - 05: Changed value from 04h to 08h and updated bit 11 description from "reserved" to "supports ONFI4.2"
  - 128: I/O pad capacitance per chip enable
  - 146-147: I/O pad capacitance, typical
  - 148-149: Input capacitance, typical
  - 150: Input pin capacitance, maximum
  - 254-255: Updated CRC values for each part number
    - Under JEDEC Parameter Page Definition table, updated the following bytes
    - 163-164: I/O pad capacitance, typical
    - 165-166: Input capacitance, typical
    - CRC
- Under Configuration Operations section,
  - Under VOLUME SELECT (E1h) subsection,
    - Updated figure to show ^{t}CSVOL spec instead of the >100ns requirement in figure
    - In paragraph 2, 2nd sentence replaced "100ns" with "^{t}CSVOL"
- Under Status Operations section,
  - In paragraph 5, changed statement to "Upon completion of the operation, the final SR[4] status and ESR flag bits should reflect any event that occurred regardless of whether it happened at the start, suspend, or resume states." from "Upon completion of the operation, the final SR[4] status should reflect any ESR flag bits event that occurred regardless of whether it happened at the start, suspend, or resume states."
- Under SLC Operations section, Under SLC/TLC Mode Operations subsection,
  - Removed statement "There are two primary methods of SLC Caching: Static and Dynamic" and removed topic heading "Static Block Usage Guidelines"
  - Removed Dynamic Block Usage Guidelines section

Rev. C – 02/12/20

- Under Package Dimensions section, updated solder ball material composition to " SACQ (92.45% Sn, 4.0% Ag, 3.0% Bi, 0.5% Cu, 0.05% Ni)" for all packages.
- Under Bus Operation - NV-DDR3 Interface section,
  - Under Differential Signaling sub-section,
    - In 4th paragraph, replaced last sentence "The differential signaling is then enabled after CE# is brought HIGH." with "The host shall then bring CE# high and wait until either ^{t}FEAT time has elapsed or the R/B# signal is back high, prior to issuing any command (including Read Status

commands) to the device. The new configuration settings shall be ready to use after either the tFEAT time has elapsed or the R/B# signal is back high."

- In the 5th paragraph, replaced last sentence "The differential signaling is then enabled after CE# is brought HIGH." with "The host shall then bring CE# high and wait until either tFEAT time has elapsed or the R/B# signal is back high, prior to issuing any command (including Read Status commands) to the device. The new configuration settings shall be ready to use after either the tFEAT time has elapsed or the R/B# signal is back high."

- Under Command Definitions section, Command Set table,
  - Added note to table and assigned to all command sets that include two command cycles. Note: "For command sets that include two command cycles where a confirm command is required, no other command is allowed between setup and confirm commands except the following:
    - RESET (FFh, FAh, FDh) commands
    - 85h can be issued between 80h/85h and 10h/15h commands

- Under Configuration Operations section,
  - Under Feature Address Details sub-section, Under Feature Address 02h: NV-DDR3 configuration table,
    - Added Note: "After a SET FEATURE (EFh) or SET FEATURE by LUN (D5h) command to Feature Address 02h, the host shall bring CE# high and wait until either tFEAT time has elapsed or the R/B# signal is back high, prior to issuing any command (including Read Status commands) to the device. The new configuration settings shall be ready to use after either the tFEAT time has elapsed or the R/B# signal is back high."
  - Under Feature Address Details sub-section, Under Feature Address DAh: Thermal Alert,
    - Added statements "Thermal Alert is evaluated for bad blocks but SR[4], ESR[1], and ESR[0] are considered invalid. For Program and Erase operations, if the operation is invalidated by Lock status (SR[7] = 0) then no Thermal Alert is evaluated." to paragraph beginning with "Thermal evaluation occurs only during valid program/read/erase operations.
- Under Status Operations section, added new paragraph
  - The Status Register flag bit SR[4] also keeps track of any Thermal Alert events during a Program, Erase, or Nested suspend/resume operations. The NAND will always check for any possible ESR Flag bit events for the duration of the operation and store SR[4] status accordingly. Upon completion of the operation, the final SR[4] status should reflect any ESR flag bits event that occurred regardless of whether it happened at the start, suspend, or resume states. This NAND behavior provides the host with critical information that may require some error handling after an operation has completed.
  - Under Status Register (SR) Definition table, Under Erase Suspend,
    - Updated "SUSPEND = 1, FAIL = 1: This state will not exist. Fail will always be "0" in Suspend State" to "SUSPEND = 1, FAIL = 1: This state will exist only for nested suspend: Erase operation suspended successfully. Following Program operation failed.
  - Under Status Register (SR) Definition table, added note to table for the SR[0] FAIL bit: "The FAIL bit is also used during DCC Training and ZQ Calibration (ZQCL, ZQCS) to feedback to the host the pass/fail result of the DCC training or ZQ calibration sequence. After the DCC training or ZQ calibration though, the NAND will remember the FAIL information prior to when the DCC training or ZQ calibration operation was run. For example, if FAIL=1 prior to enabling DCC training via FA:20h P1[0]=1, if DCC training completed successfully then a Read Status while in DCC training mode (FA:20h P1[0]=1) will return FAIL=0, however after the DCC training mode is exited (FA:20h P1[0]=0), a succeeding Read Status will return FAIL=1 which was the previous value of the FAIL bit prior to the DCC training. For a ZQ Calibration operation, if FAIL=1 (due to program failure of Program N-1) prior to the ZQ Calibration operation, then if the ZQ Calibration was successful, a Read Status will return FAIL=0 reflecting that the ZQ Calibration operation was successful,

however if a Program N operation is issued immediately afterwards, and Program N was successful, then FAIL=0 (reflecting Program N was successful), but FAILC=1 (reflecting that Program N-1 had failed)."

- Under Read Operations section, Read Offset Prefix (2Eh) Command subsection,
  - Update figures "Read Offset Prefix (2Eh) Command with Read Page (00h-30h) with ACRR Enabled", "READ OFFSET PREFIX (2Eh) Command with IWL READ (00h-20h) with ACRR Enabled", "READ OFFSET PREFIX (2Eh) Command with SLC OTF with ACRR Enabled"
    - In the Read Offset Prefix Command changed "Offset" to "Address" for the 3 address cycles
    - Updated DQ[7:0] color to match address cycle for Read Voltage Offset 1-3
  - Under Example Sequence for Clearing Read Offsets,
    - Moved "Offsets are cleared" from step 4 to step 5.
  - Under Valid Commands and Feature Addresses table, removed Not Valid entries
- Under IWL READ (00h-20h) section,
  - Under Read Offset Restriction, removed P3 from statement: "FEATURE ADDRESS A0h-ABh Subfeatures P1/P2/P3 are read only with GET FEATURE (EEh), the values will only be set when using READ OFFSET PREFIX (2Eh) Command."
  - Under Read Feature Compatibility Table, Changed Column header of "Different Offset Values Allowed on Different Planes?" to "Different Offset Values Allowed on Different Plane Groups?"
  - Under IWL Restrictions, Status Register subsection,
    - In restriction starting with "IWL Read has unique status register bits SR[6] and SR[5]...., replaced "the user must issue a READ STATUS (70h) command," with "the user must issue a READ STATUS (70h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command,"
- Under Read Operations section, Single Bit Soft Bit Read Operations subsection,
  - In Definitions for Feature Addresses B1h-B4h, E1h-E3h table, changed Feature Address E3h Subfeature Parameter P4 from "Negative SBSBR Offset for SLC only pages" to "Positive SBSBR Offset for SLC only pages"
- Under SLC Operations section,
  - Under Prefix Opcode for SLC Entry subsection,
    - Update figure "READ OFFSET PREFIX (2Eh) SLC OTF Sequence"
- In the Read Offset Prefix Command changed "Offset" to "Address" for the 3 address cycles
- Updated DQ[7:0] color to match address cycle for Read Voltage Offset 1-3
  - Under Valid Operations with SLC MODE LUN ENABLE (3Bh) table, removed Status Operation from table as it is Invalid.
- Under TLC One Pass Programming section,
  - Under PROGRAM SUSPEND (84h) and PROGRAM RESUME subsection,
    - Under SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands are permitted during program suspend (including nested suspend), to the following feature addresses,
- Added Feature Address 84h: Clear Extended Status Register
    - Update paragraph from " If the host issues a PROGRAM SUSPEND (84h) while there is no program operation ongoing the command should be ignored (i.e. ^{t}PSPD = 0, R/B# stays HIGH). If the host issues a PROGRAM RESUME (13h) while there is no program operation ongoing or no program suspended, the NAND will respond with a ^{t}PSPDN busy time and the LOCK status (SR[7]=0) is set (SR[3], SR[2], SR[1], and SR[0] will be "don't care"). If the host issues a PROGRAM SUSPEND (84h) to a LUN already in program suspend state the NAND will respond within ^{t}PSPDN busy time and the program that was suspended will stay in the program suspend state." to " If the host issues a PROGRAM SUSPEND (84h) while there is no program operation ongoing

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the command should be ignored (i.e. ^{t}PSPD = 0, R/B# stays HIGH). If the host issues a PROGRAM RESUME (13h) while there is no program operation ongoing or no program suspended, the NAND will respond with a ^{t}PSPDN busy time and the LOCK status (SR[7]=0) is set (SR[3], SR[2], SR[1], and SR[0] will be "don't care"), SR[4] is reset, ESR[1] and ESR[0] will not change. If the host issues a PROGRAM SUSPEND (84h) to a LUN already in program suspend state the command will be ignored and the program that was suspended will stay in the program suspend state."

- Under Erase Operations section, ERASE SUSPEND (61h) and ERASE RESUME subsection,
  - Added ", SR[4] is reset, ESR[1] and ESR[0] will not change." to the statement "If the host issues an ERASE SUSPEND (61h) command while there is no erase operation ongoing the command should be ignored (i.e. ^{t}ESPD = 0). If the host issues an ERASE RESUME (D2h) command while there is no erase operation ongoing or no erase suspended, the NAND will respond with a ^{t}ESPDN busy time and the LOCK status (SR[7]=0) is set (SR[3],SR[2], SR[1], and SR[0] will be "don't care"), SR[4] is reset, ESR[1] and ESR[0] will not change."
  - In ERASE SUSPEND (61h) Status Details table, added note to ERASE suspended of "See Nested Suspend section for status details during nested erase suspend."

- Under Electrical Specifications - Array Characteristics section, TLC and SLC Array Characteristics table
  - Update ^{t}RSPSPD (Min) = 325us to^{t}RSPSPD (Min) = 200us in Note 9 for TLC Array Characteristics table only.
  - Update Parameter for ^{t}ESPDN from "Busy time when ERASE SUSPEND is issued when LUN is already in the suspend state or ERASE RESUME is issued when no erase is suspended or ongoing" to "Busy time when ERASE RESUME is issued when no erase is suspended or ongoing." for TLC and SLC table.
  - Update Parameter for ^{t}PSPDN from "Busy time when PROGRAM SUSPEND is issued when LUN is already in the suspend state or PROGRAM RESUME is issued when no program is suspended or ongoing" to "Busy time when PROGRAM RESUME is issued when no program is suspended or ongoing." for TLC and SLC table.

Rev. B – 11/20/19

- Under Signal Assignments section,
  - Update 132-ball BGA (Ball-Down, Top View) figure to have 4 CE
  - Removed note: These signals are available on 16 LUN stacked packages. They are NC for other configurations.

- Under Read Operations section,
  - Under IWL READ (00h-20h) section,
    - Removed statement: "If the column byte address specified by the IWL Read is part of the second 4KB+ section of the page (bytes 4588 - 9175) ^{t}RSNAP will be ~ 2.5µs longer than the ^{t}RSNAP TYP."
- Under TLC One Pass Programming section,
  - Under PROGRAM SUSPEND (84h) and PROGRAM RESUME (13h) subsection,
    - Change statement "SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands are permitted during program suspend." into own section titled "SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands are permitted during program suspend (including nested suspend), to the following Feature Addresses: " and provided list of feature addresses that are allowed.
- Under Multi-Plane Operations section, under Multi-Plane addressing
  - Added "multi-plane" to statement: "The LUN address bit(s) must be identical for all of the issued multi-plane addresses."

  - Replaced statement "The plane select bits, PS[13:12] must be different for each issued address, but each plane address can be issued (queued) in any order." with the following two statements: "Each plane address can be issued (queued) in any order." and "Re-issuing a multi-plane program operation to the same plane is allowed prior to the program confirm command (10h/15h). However, this condition requires all addresses and data input to be identical to the previous operation to that plane."

- Under Electrical Specifications - Array Characteristics section,
  - Update TLC Array Characteristics table Dummy busy time ^{t}DBSY Max value to 0.5us from 1us.

Rev. A – 11/04/19

- Initial release